

NOTE: THIS BUG. S/B  
ENHANCED, AS PER,  
EG. 6, 055, 295

RADIATION GENERATION  
SYSTEM

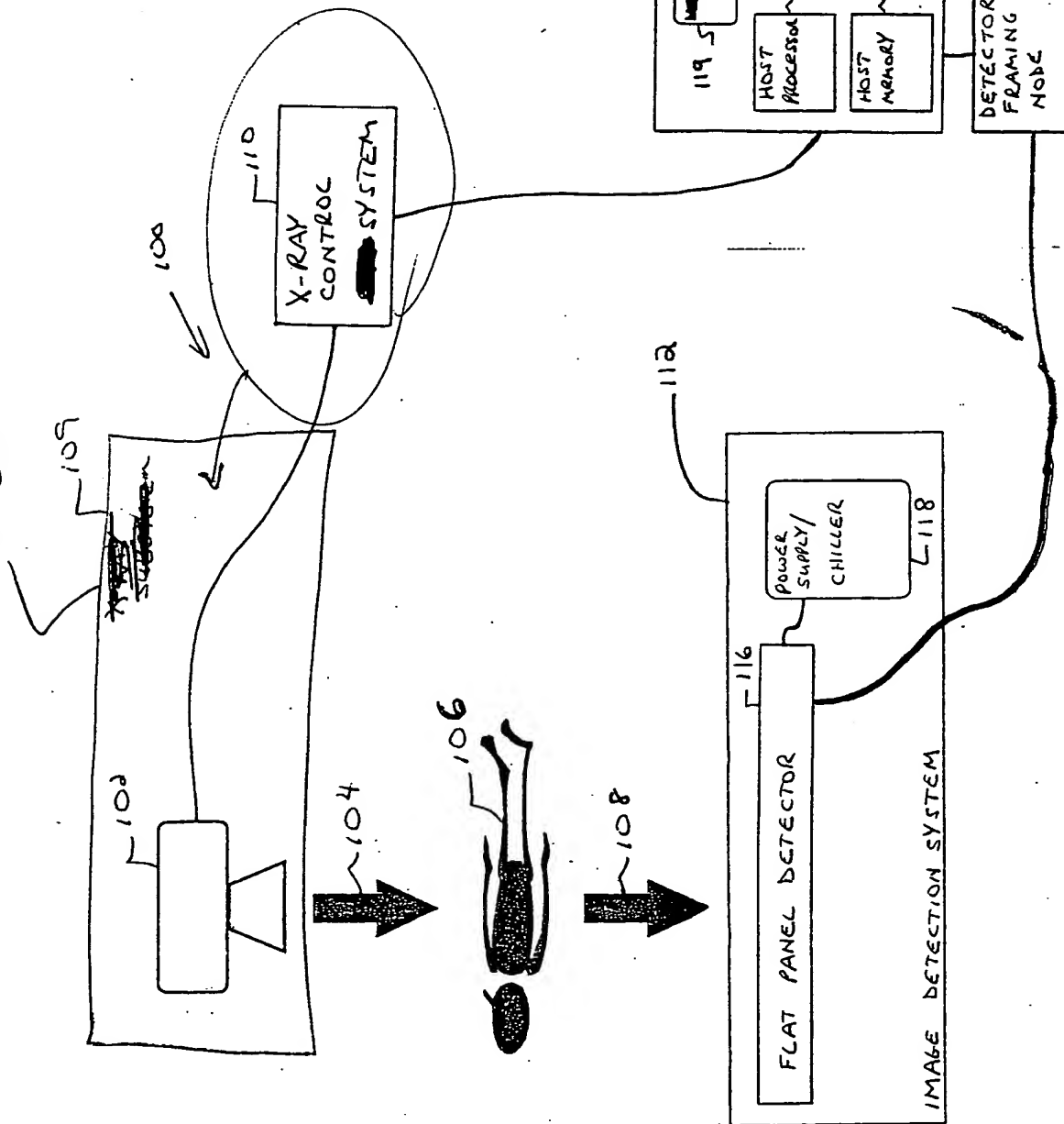


FIG. 1

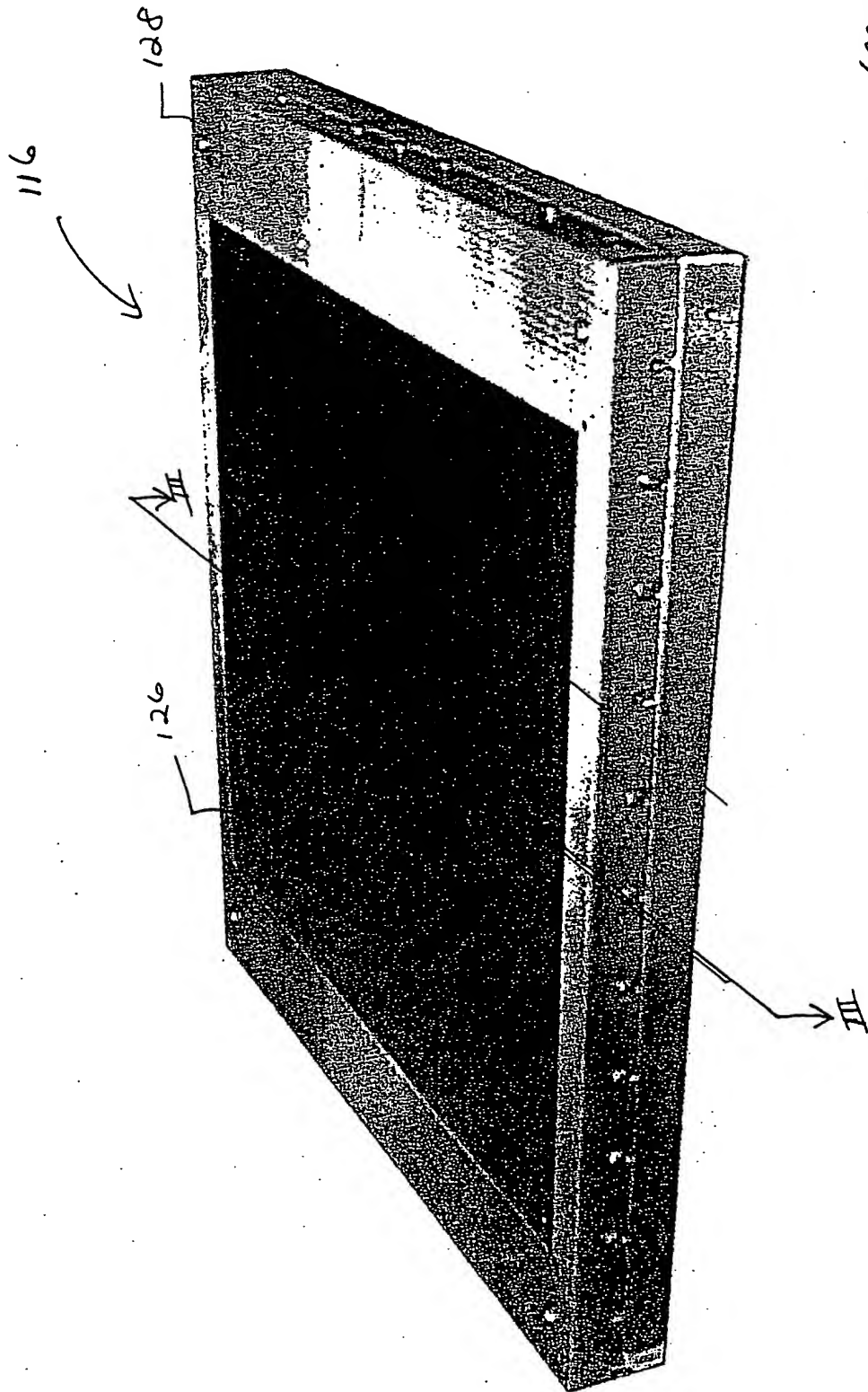


FIG. 2 (PRIOR ART)

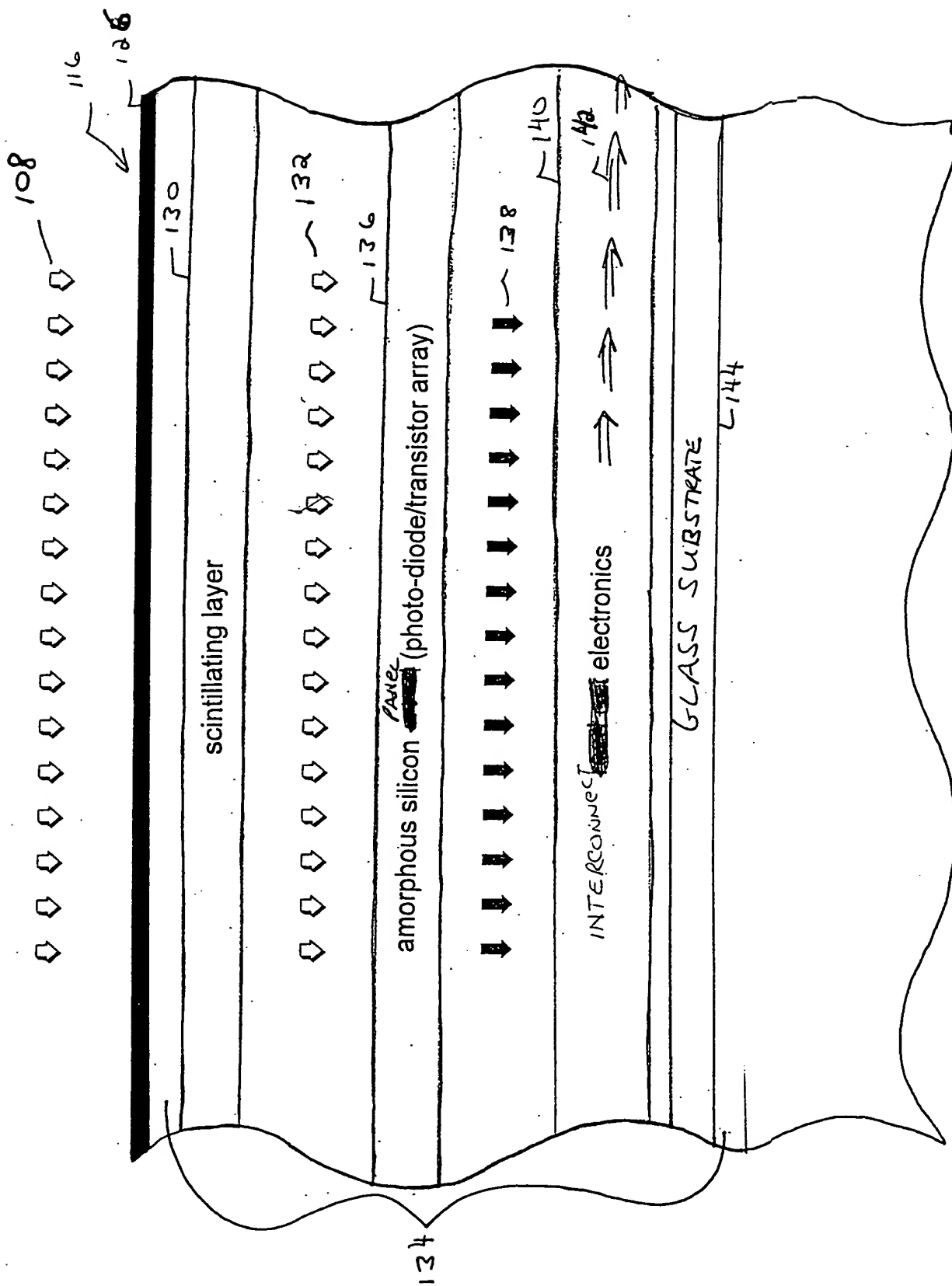


FIG. 3

FIG. 4 is a perspective view of a prior art device. The device includes a base 130, a top surface 134, and a side surface 136. A grid 144 is disposed on the top surface 134. A curved surface 146 is disposed on the side surface 136. A grid 150 is disposed on the curved surface 146. A grid 148 is disposed on the base 130.

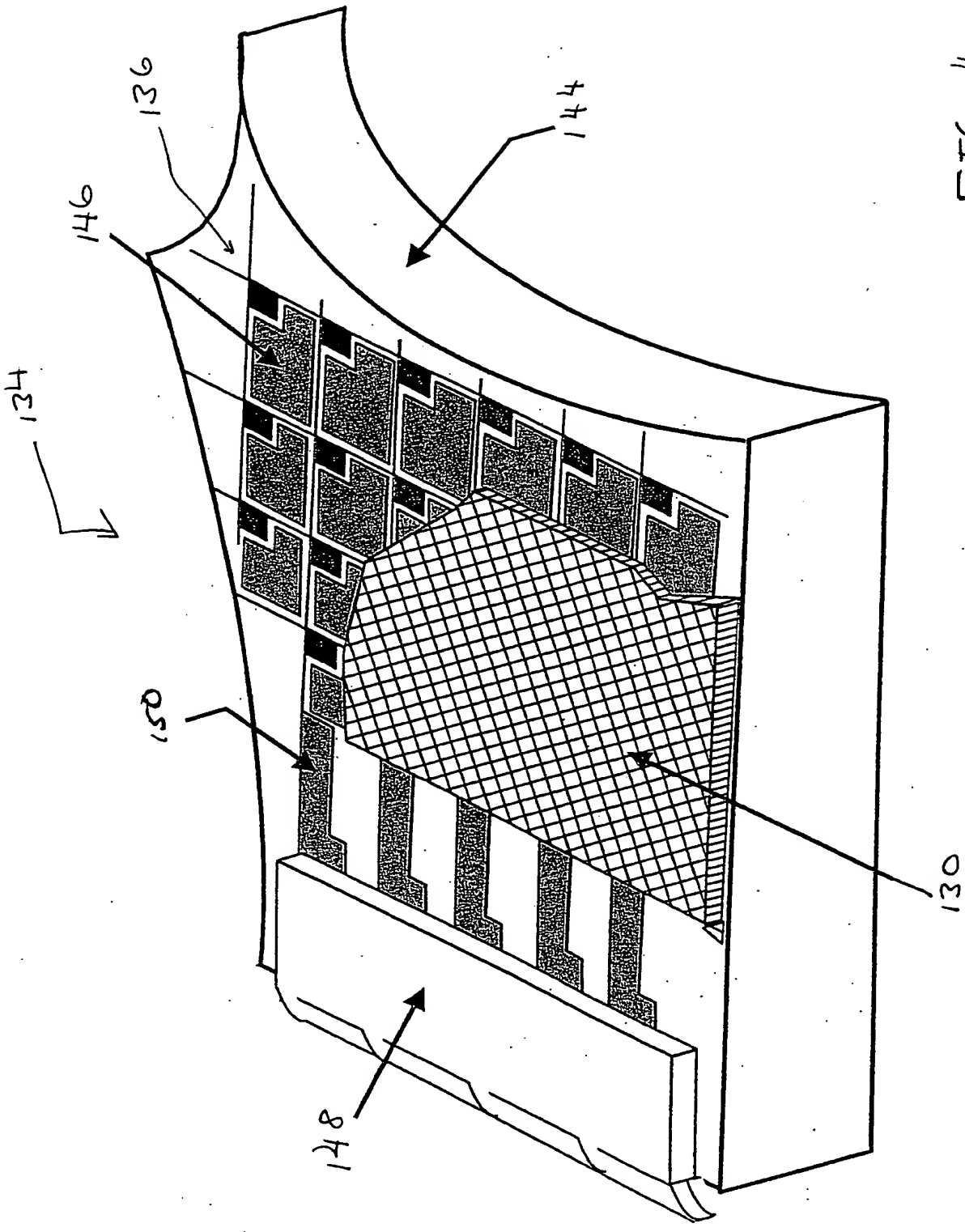


FIG. 4  
(PRIOR ART)

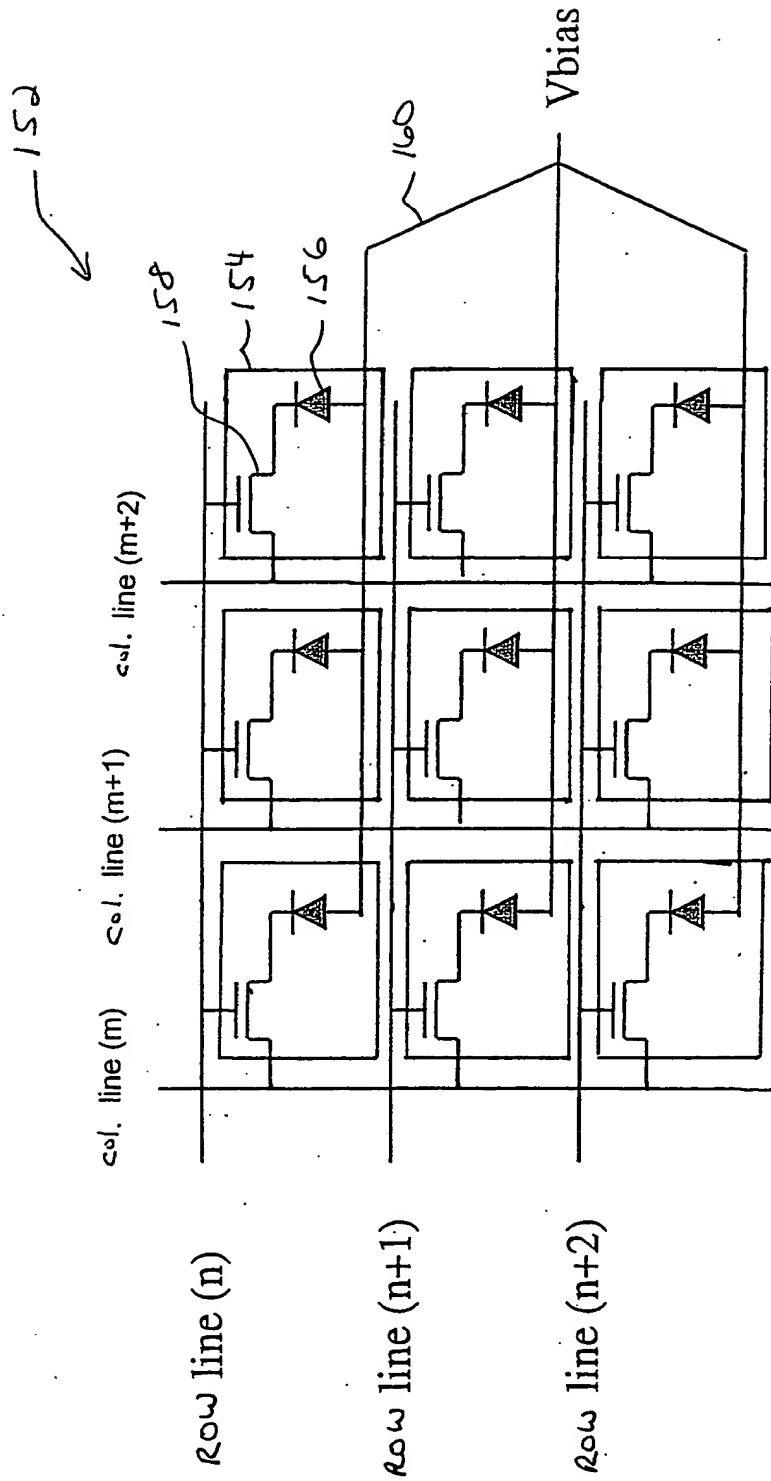


FIG. 5  
(Prior Art)

FLAT PANEL DETECTOR

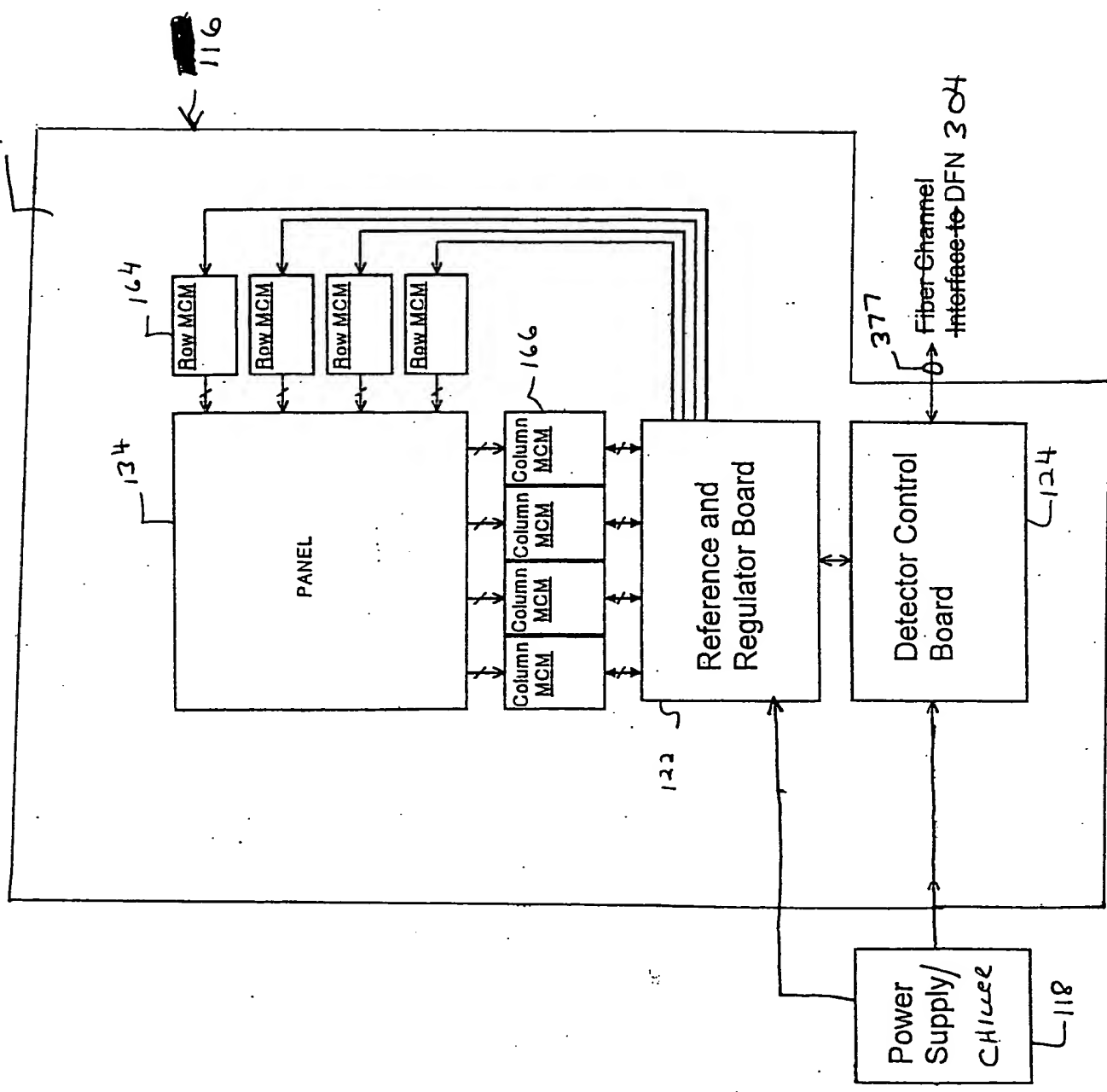


FIG. 6  
(PRIOR ART)

FLAT PANEL DETECTOR

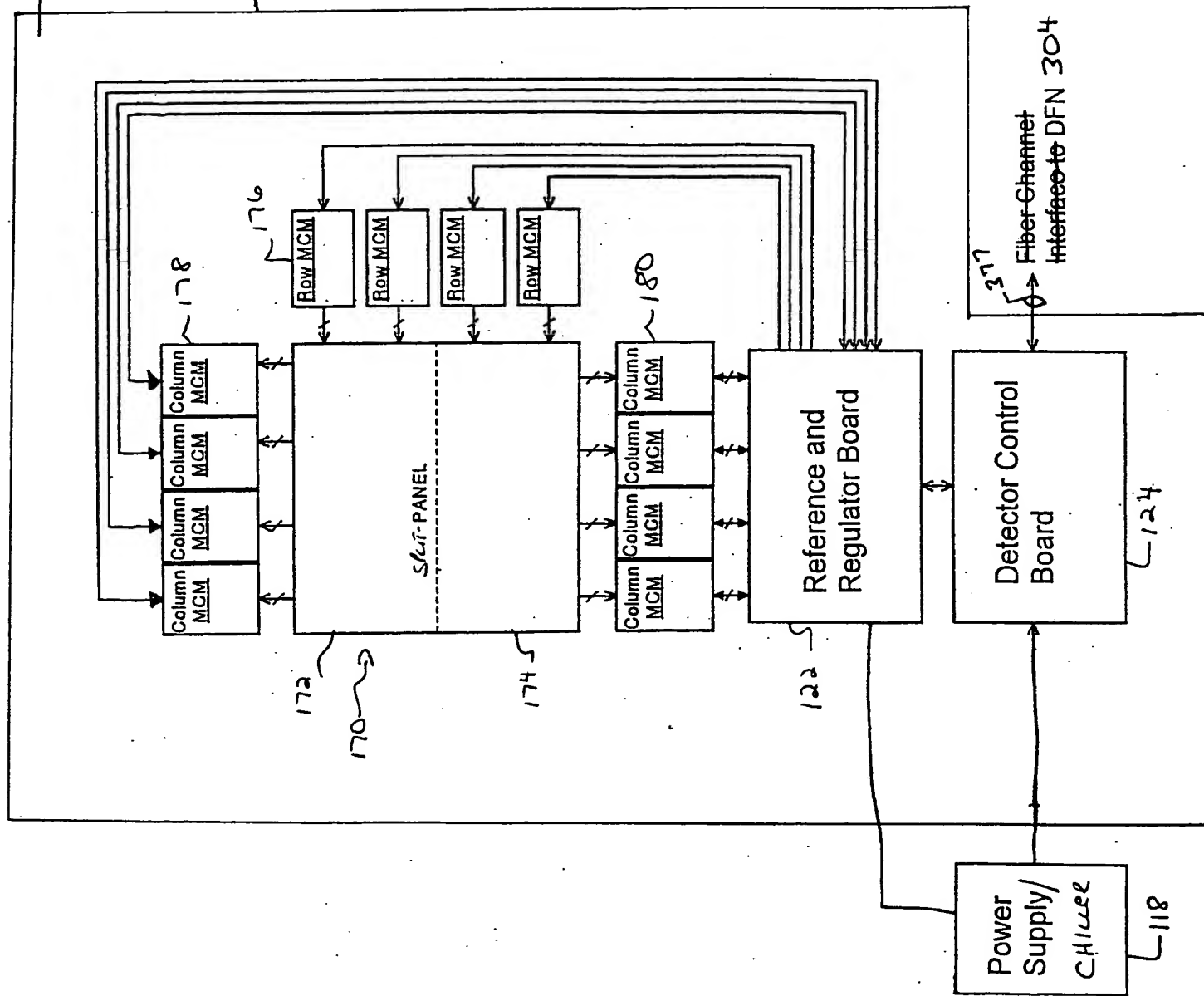
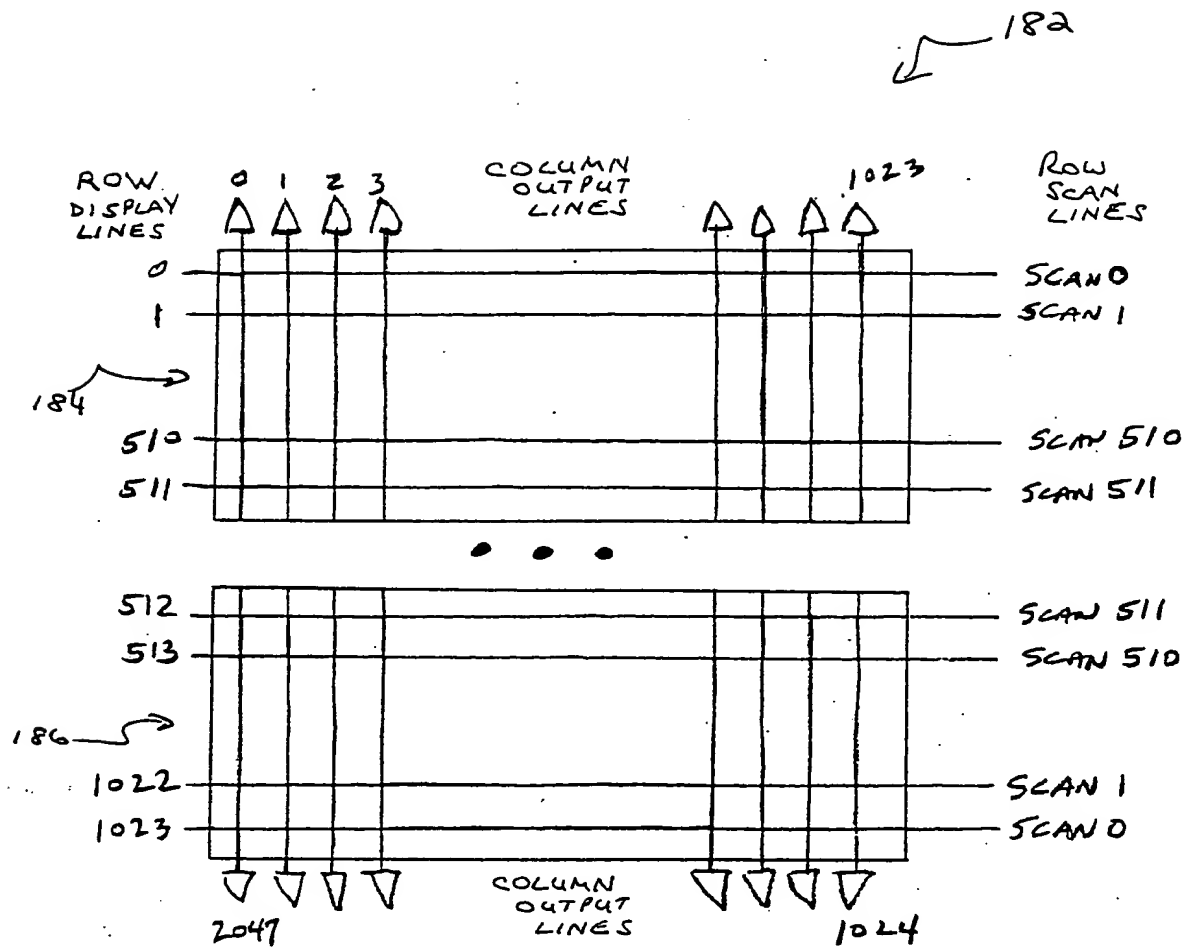


FIG. 7  
(PRIOR ART)



CARDIAC/SURGICAL DIGITAL X-RAY PANEL

FIG. 8  
(PRIOR ART)



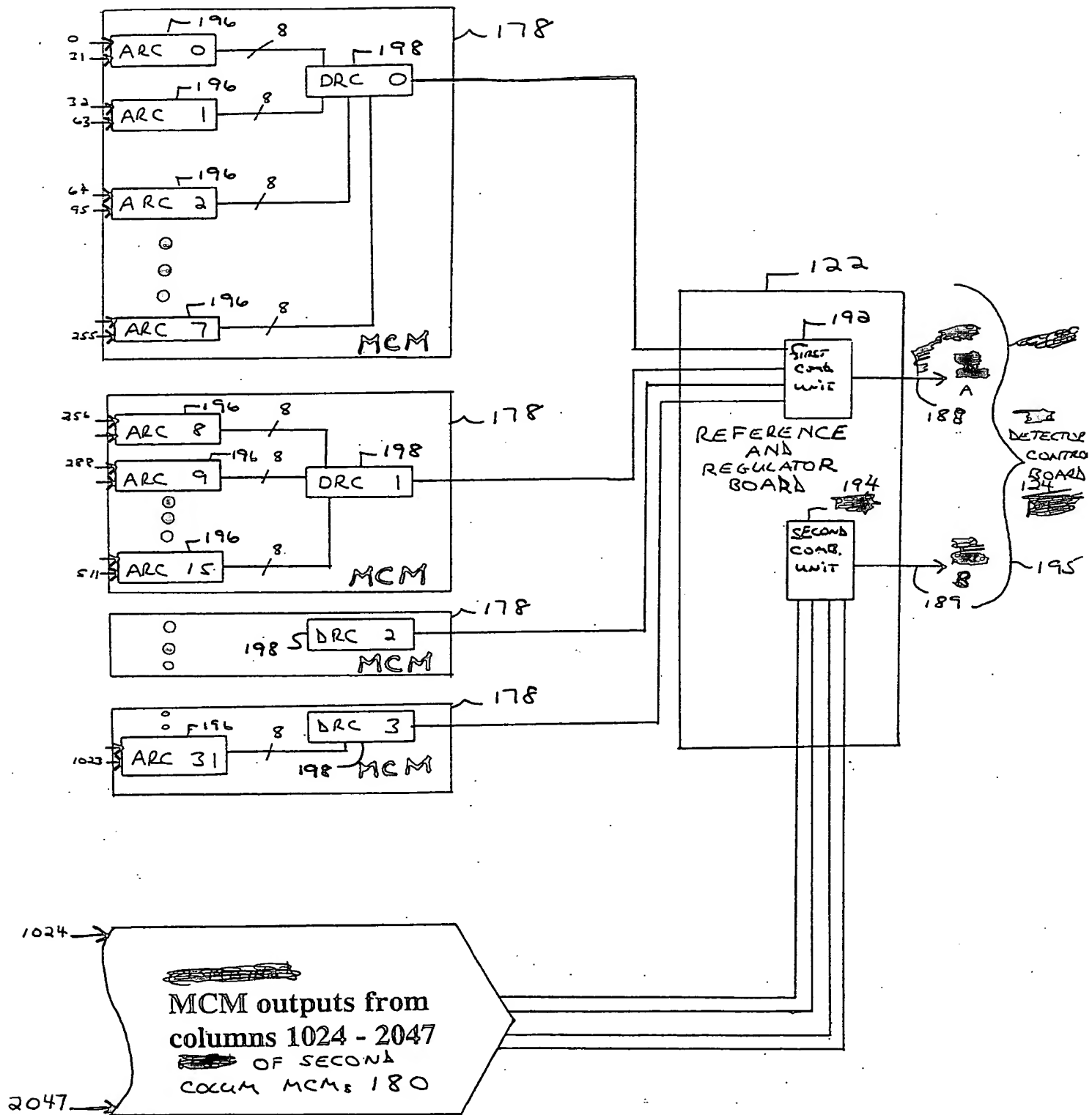
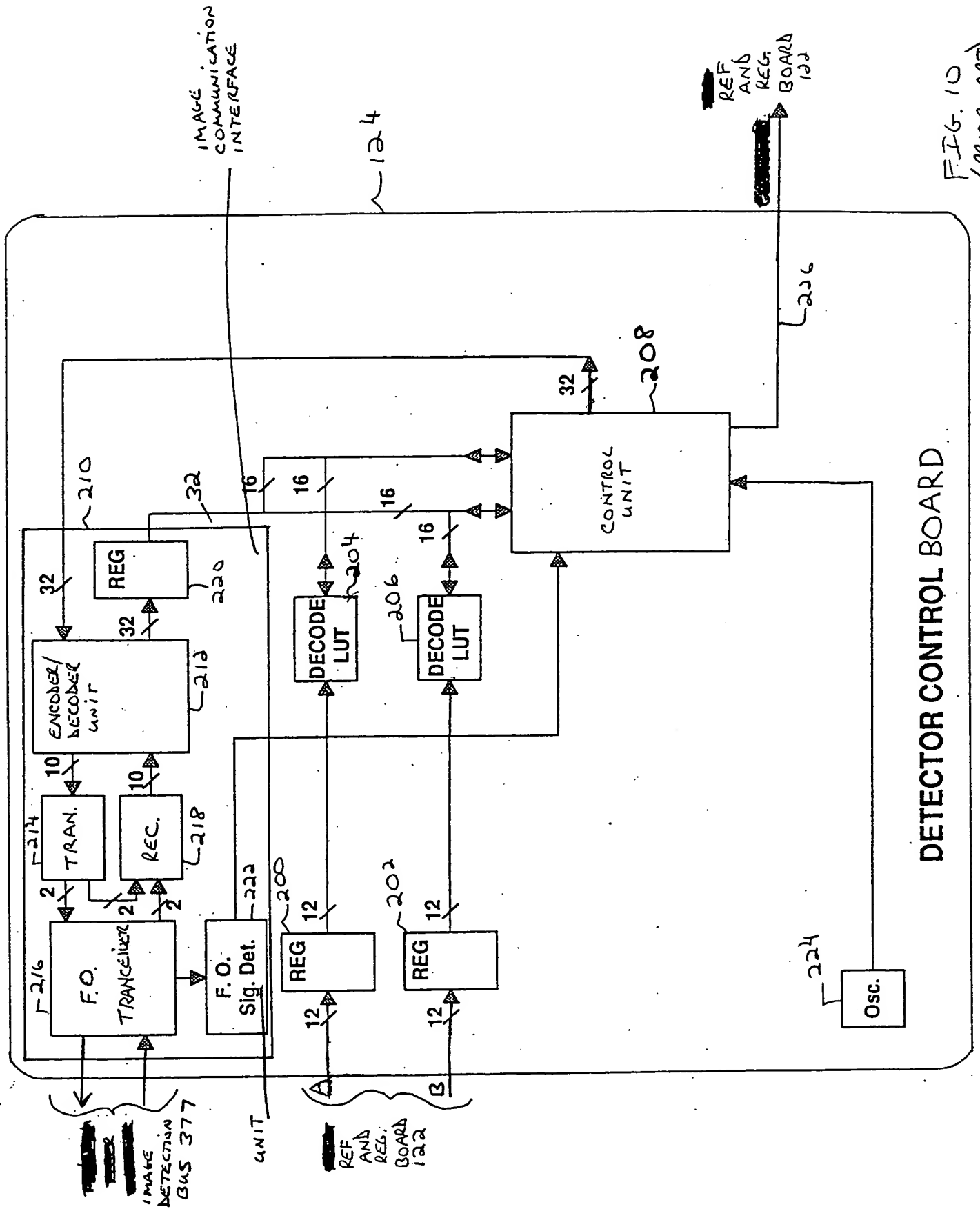


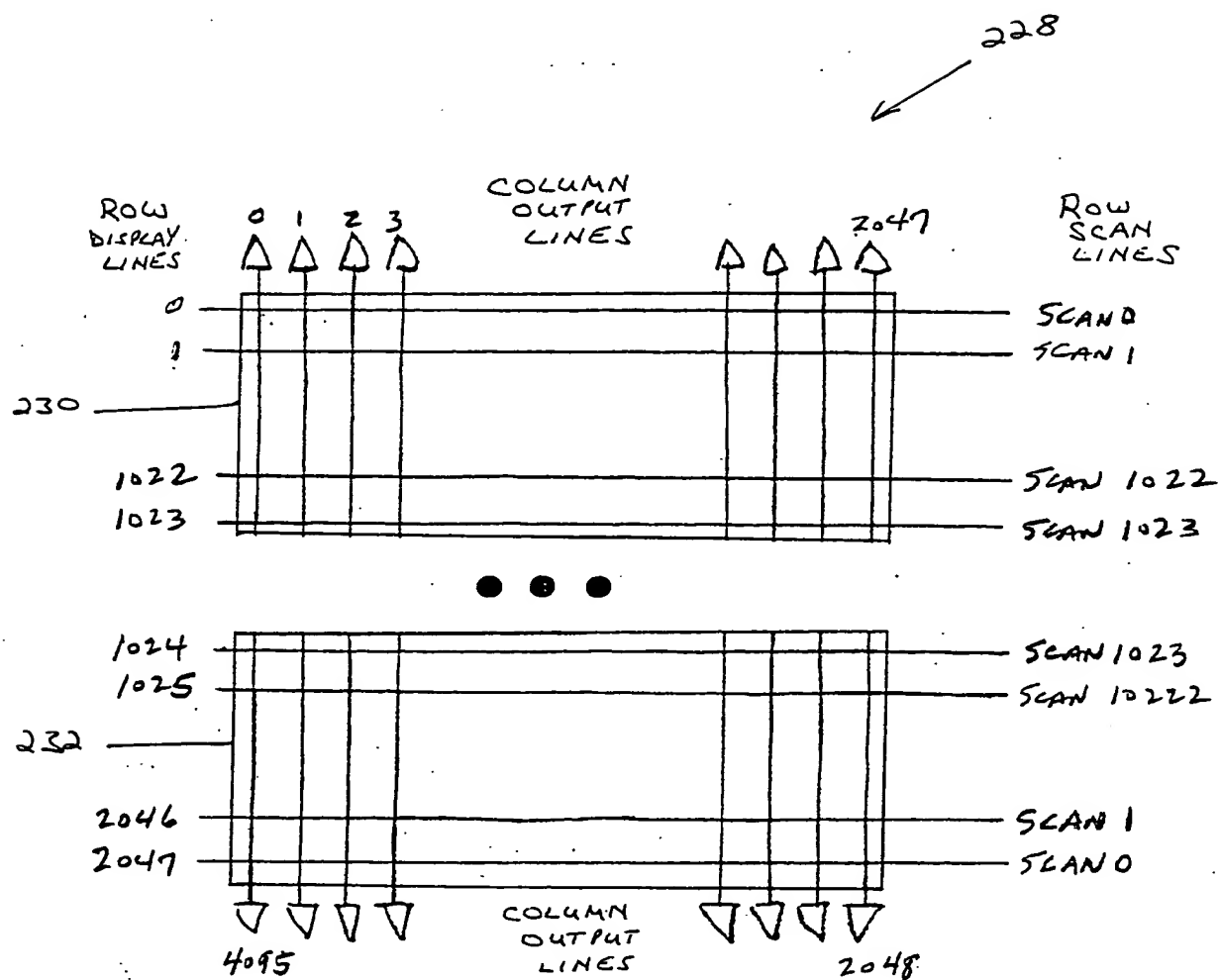
FIG. 9  
(PRIOR ART)

FIG. 10 is a block diagram of a detector control board.



DETECTOR CONTROL BOARD

FIG. 10  
(PRIOR ART)



RADIOGRAPHY DIGITAL X-RAY PANEL

FIG. 11  
(PRIOR ART)

1. The present invention relates to a flat panel detector system and more particularly to a flat panel detector system with a reference and regulator board and a detector control board.

FLAT PANEL DETECTOR

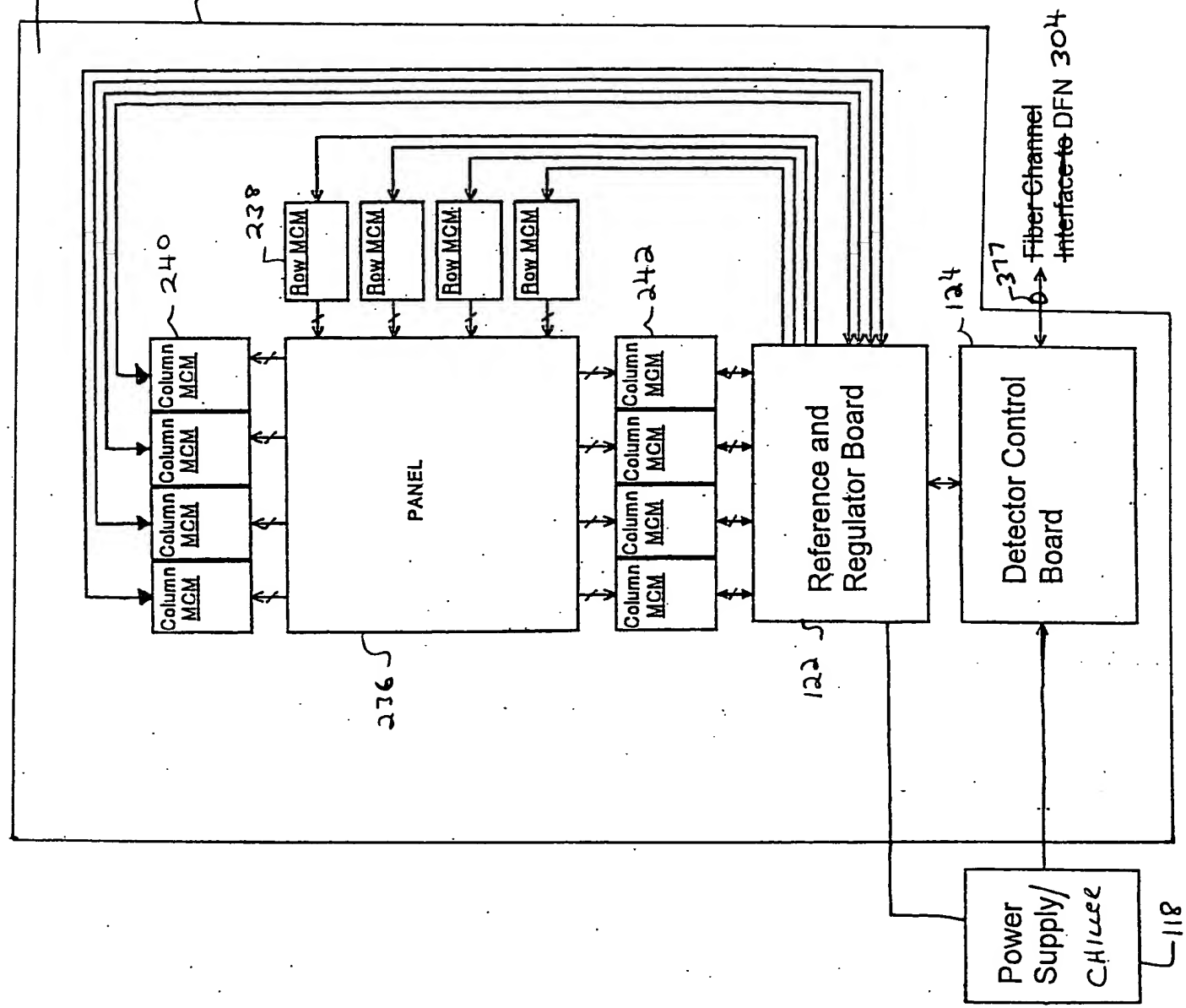


FIG. 12  
(Prior Art)



FLAT PANEL  
DETECTOR

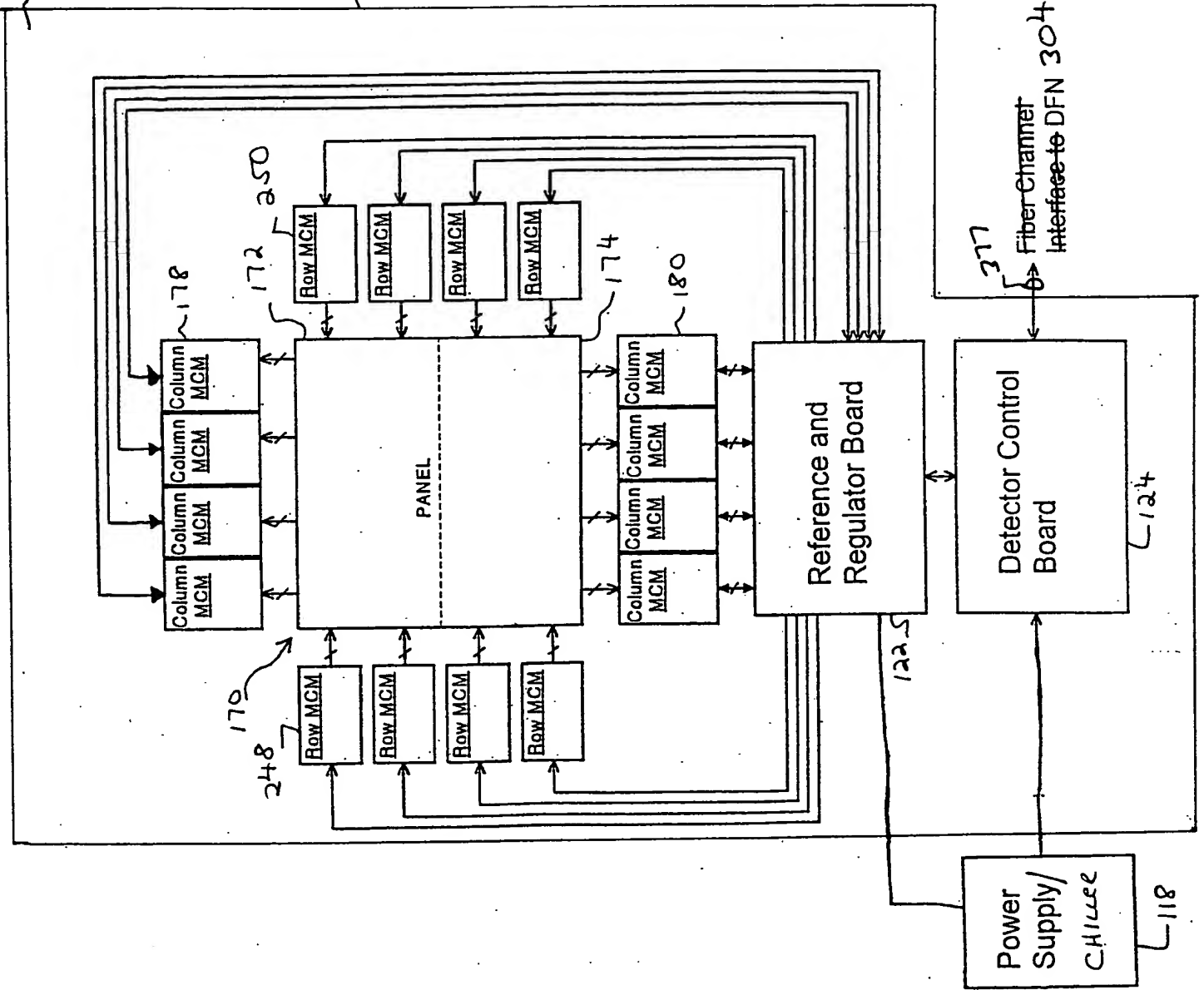


FIG. 14  
(PRIOR ART)

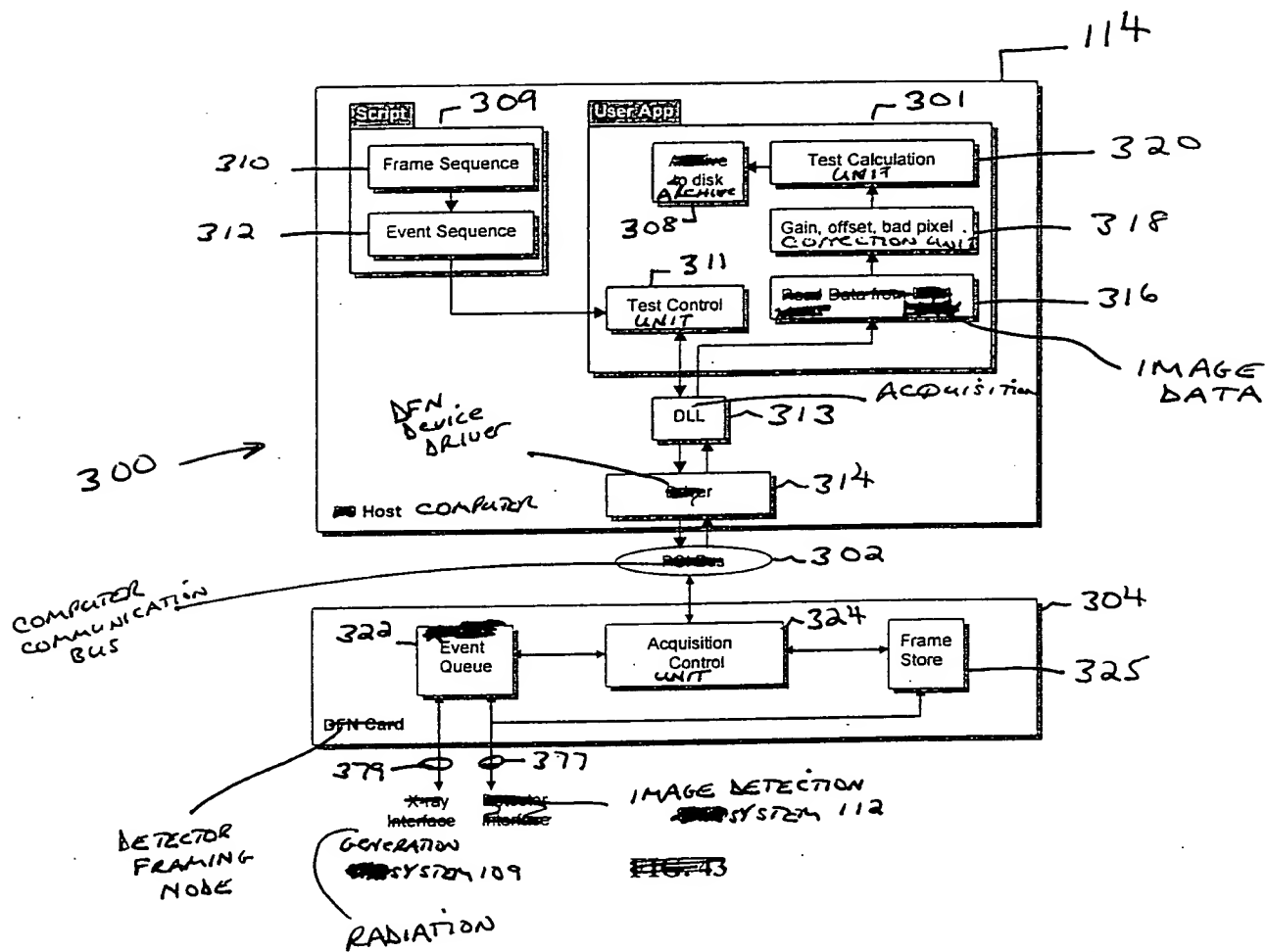


FIG. 15

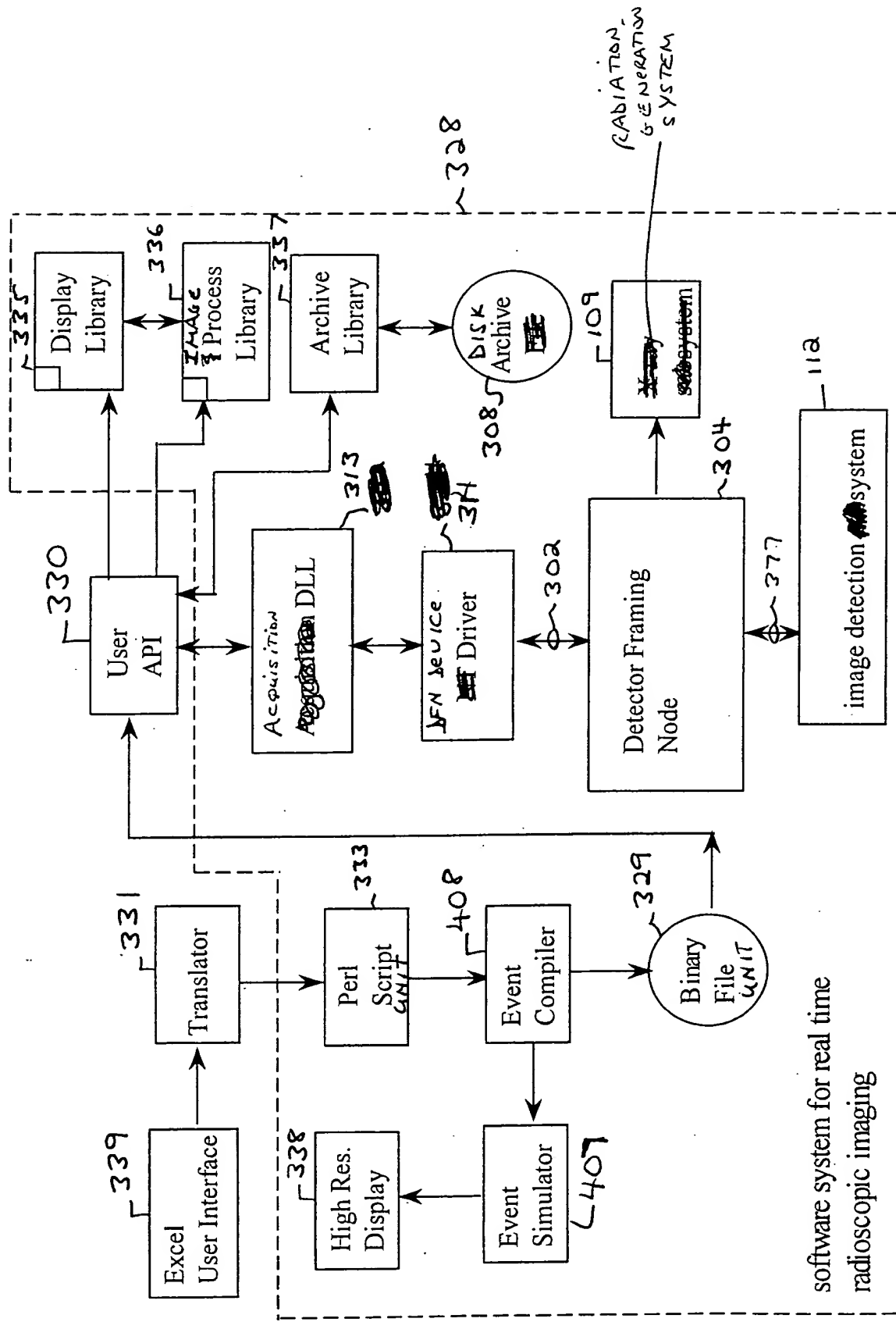


FIG. 16



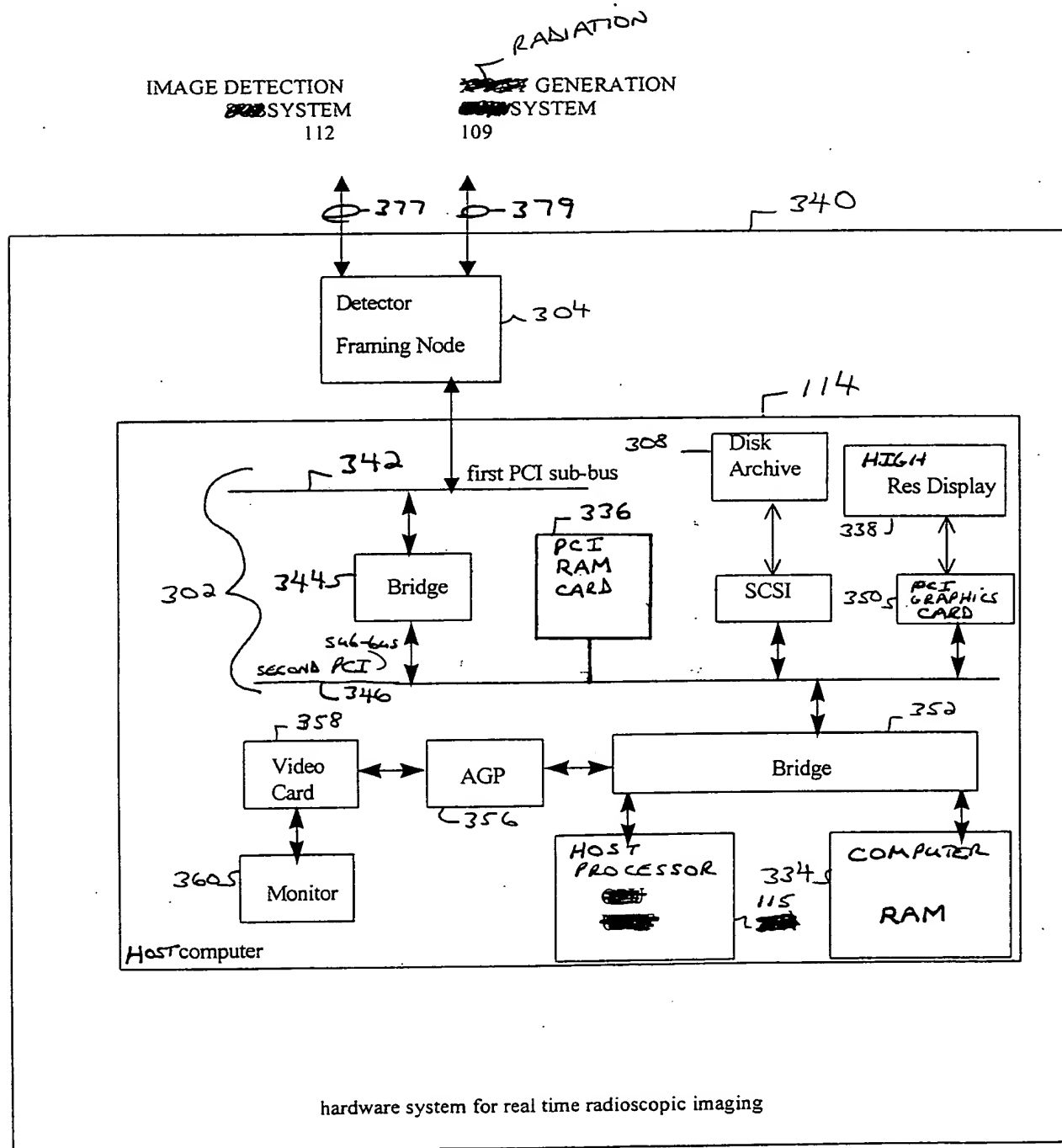


FIG. 17

1.2

FRAME BUFFER MEMORY

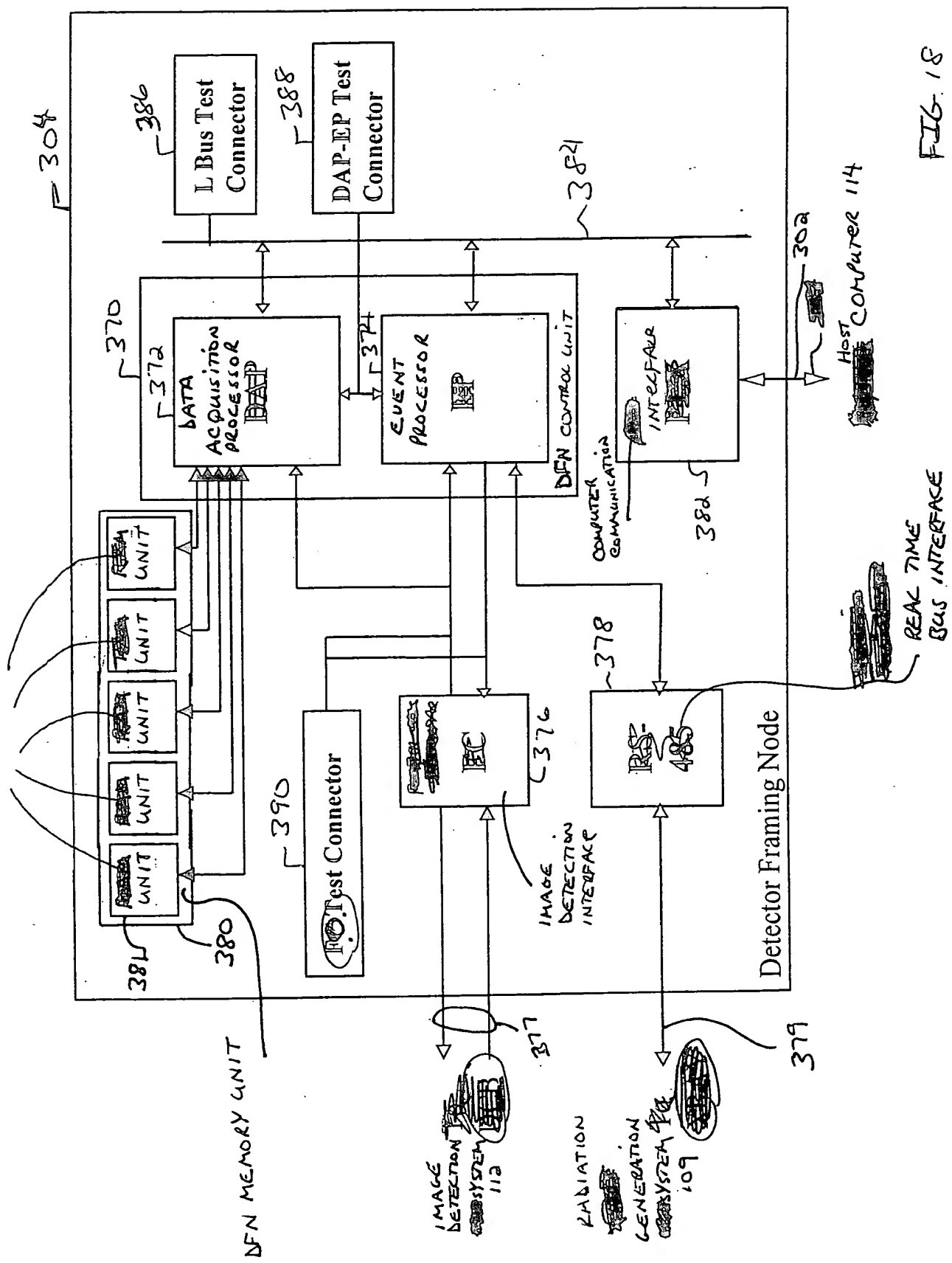


FIG. 18

Panel Setup	Real Time	(fm/sec)	length	Latency	memory	offset	gbr
Single Frame	Post Process	30	unlimited	< 5 frames	host	none	
Single Frame	Post Process	-	-	Delay ~.1 sec	"	y	
Single Frame	Post Process	-	-	Delay ~.2 sec	"	y	y
Real Time	Real Time	R	Unlimited	< 5 frames	host	none	
Real Time	Real Time	R - X	Unlimited	< 5 frames	"	y	
Real Time	Real Time	R - Y	Unlimited	< 5 frames	"	y	y

FIG-19

Modality	Image size	Frames Stored
Cardiac	1024 x 1024	host memory
Rad	2048 x 2048	200
Mammo	2304 x 2048	50
		44

FIG. 20

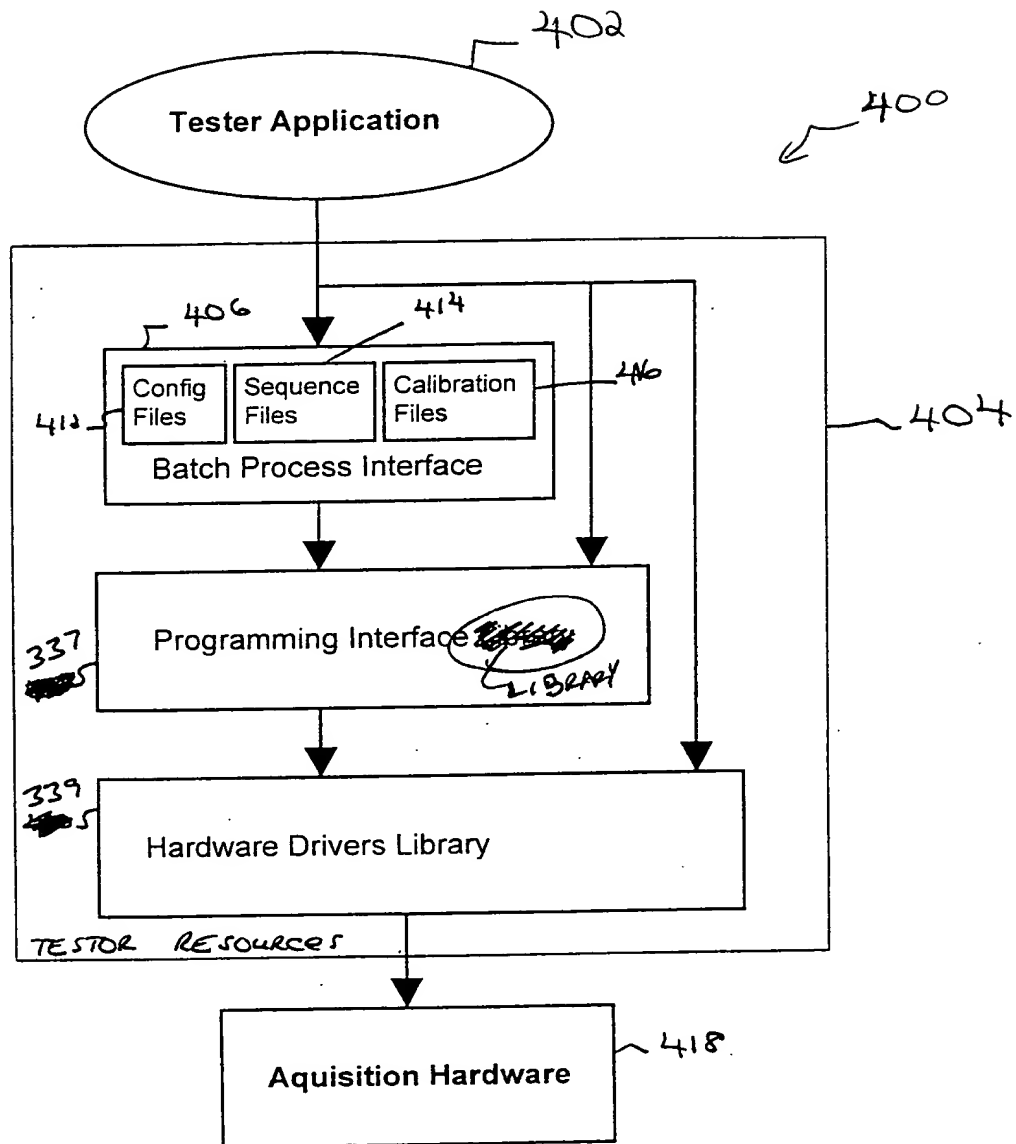


FIG. 21

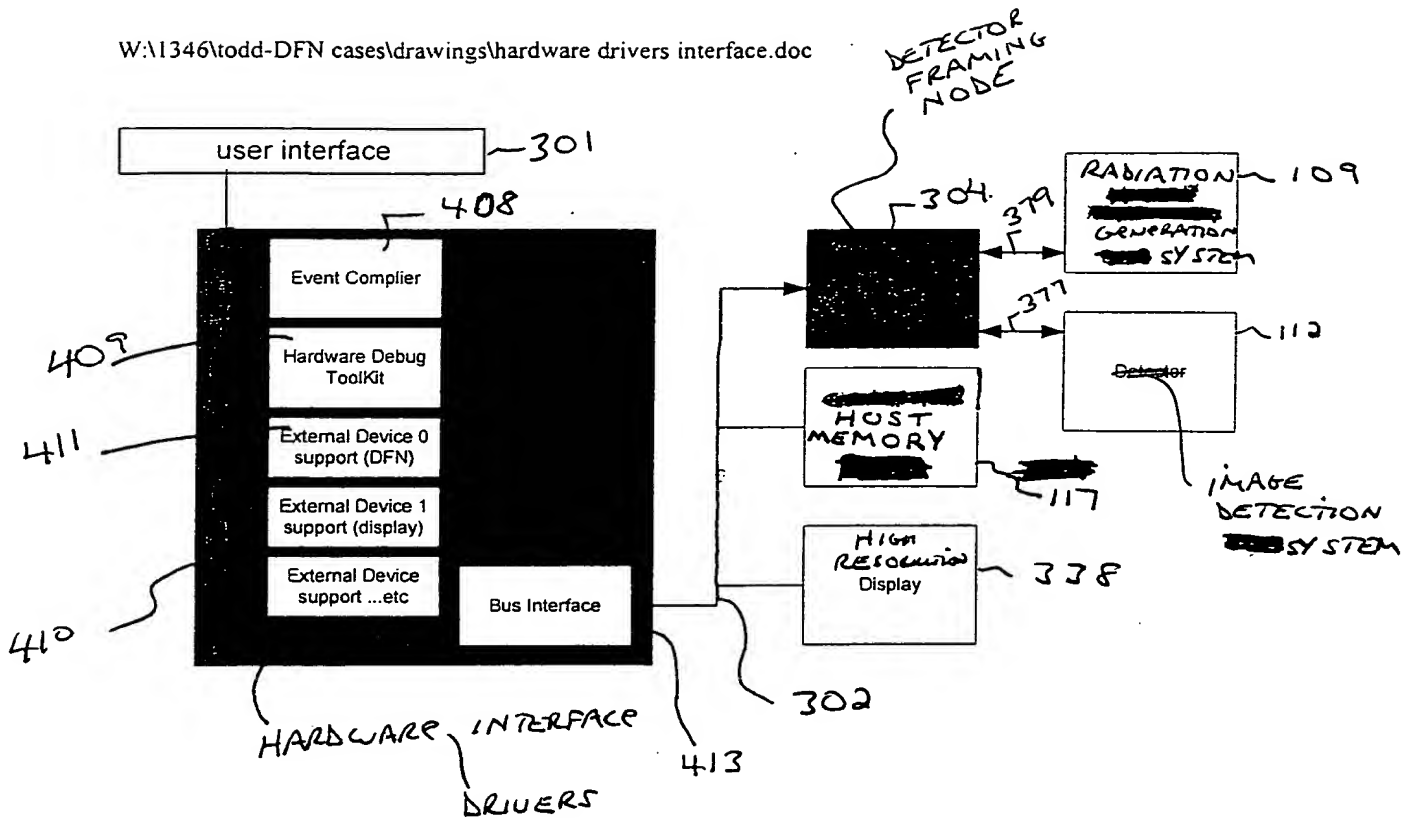


FIG. 22

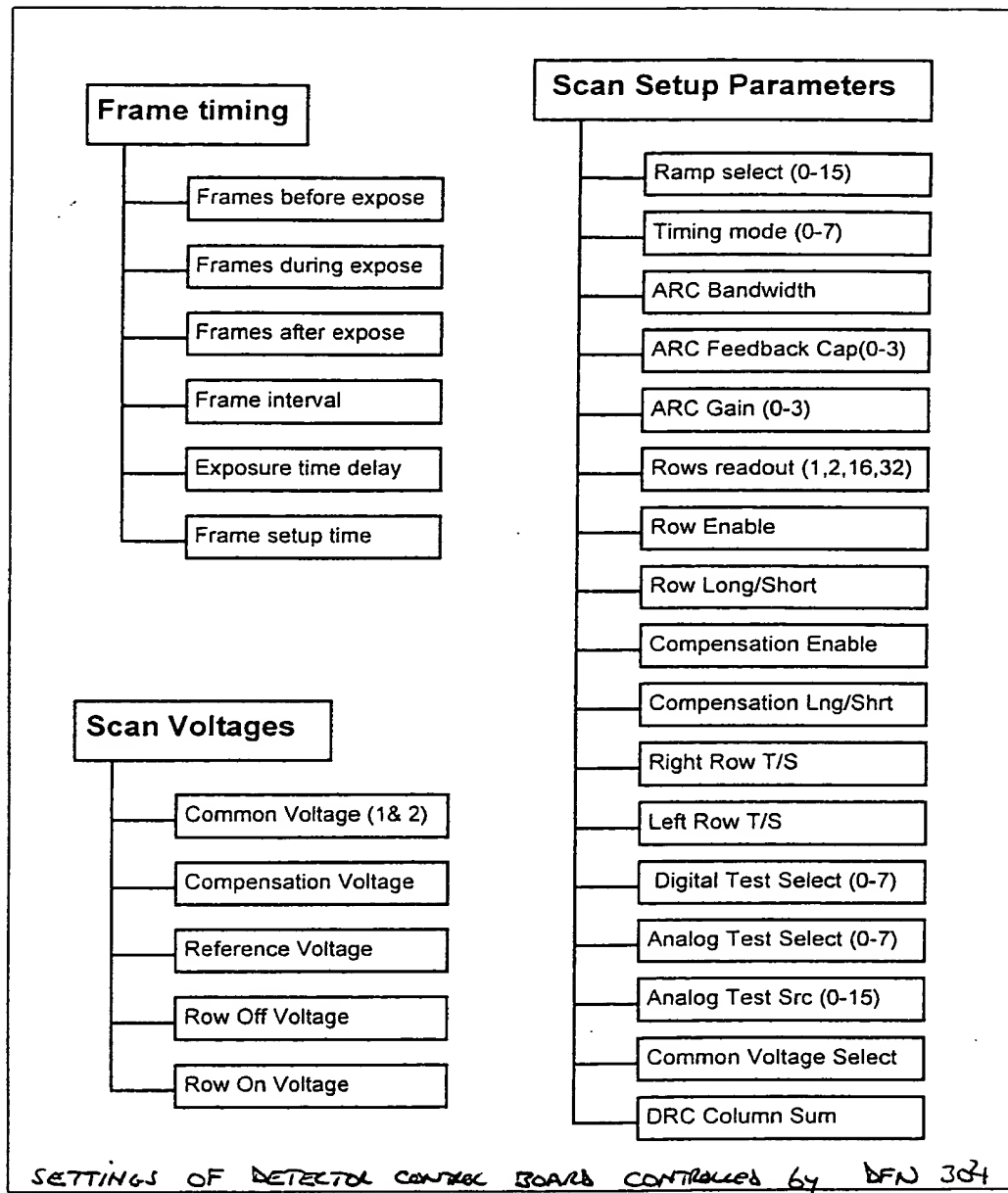


FIG. 23

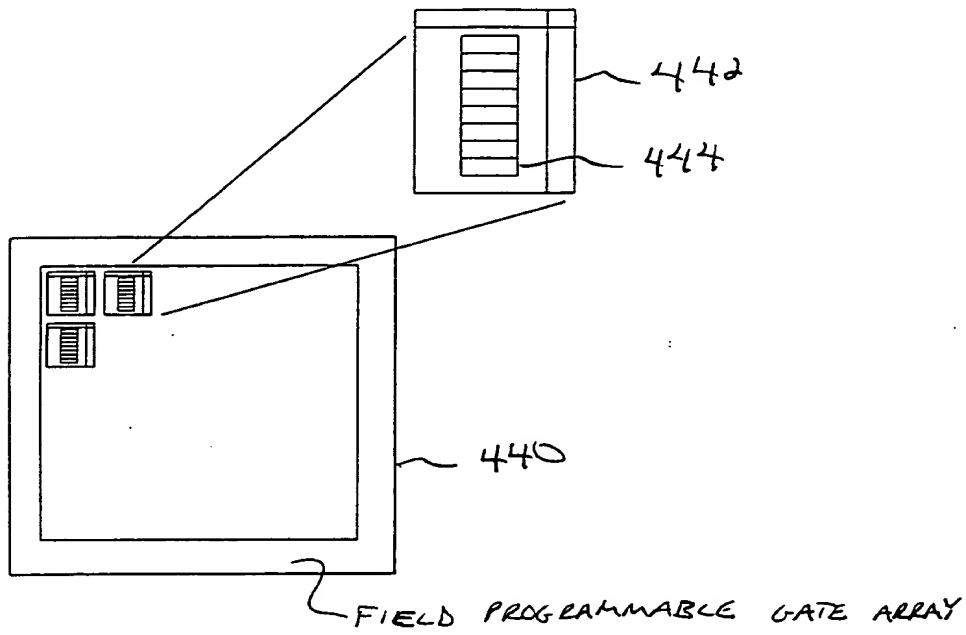


FIG. ~~23~~ 24

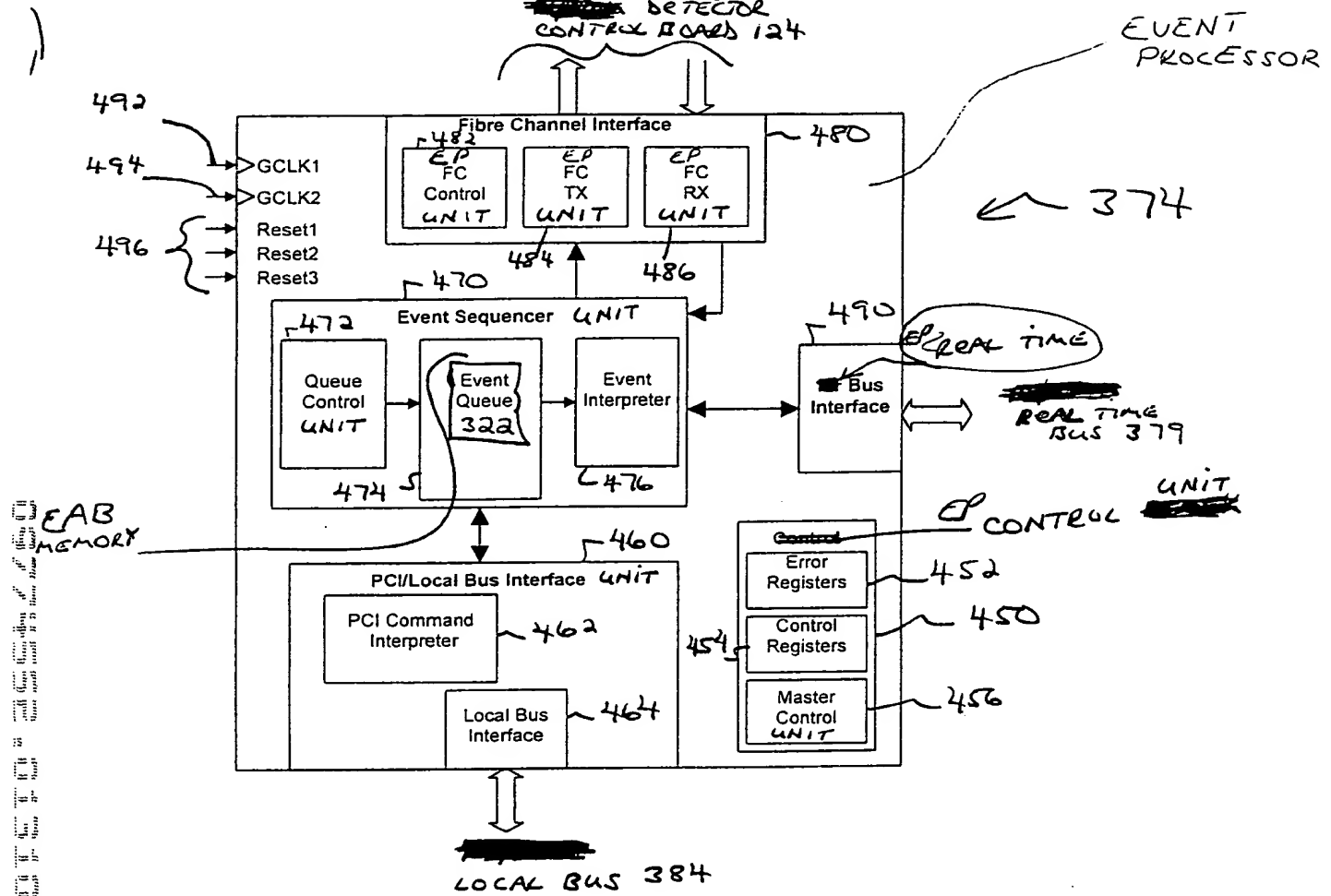


FIG. 25



IMAGE  
DETECTION  
BUS  
377

DATA ACQUISITION PROCESSOR

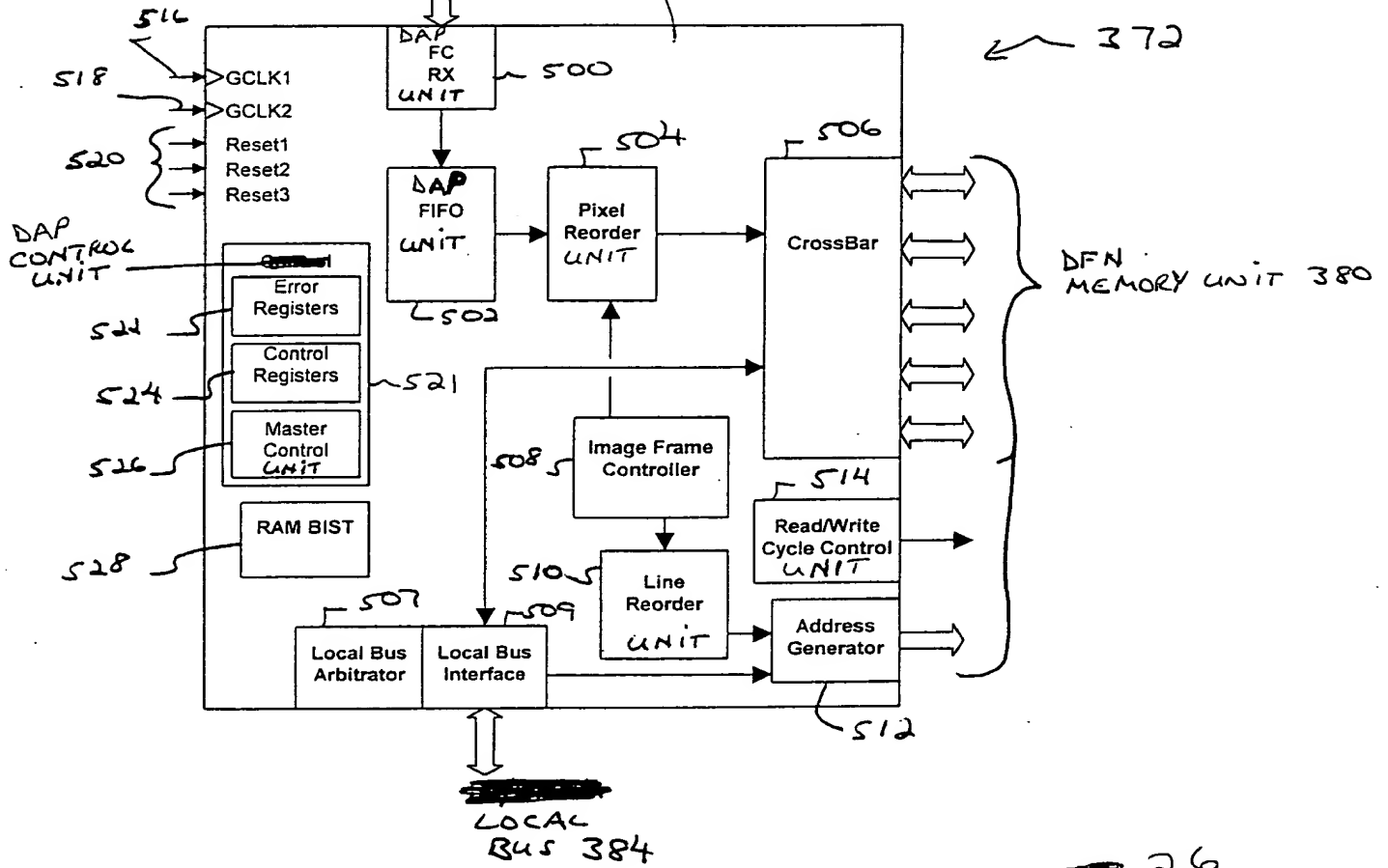


FIG. 26

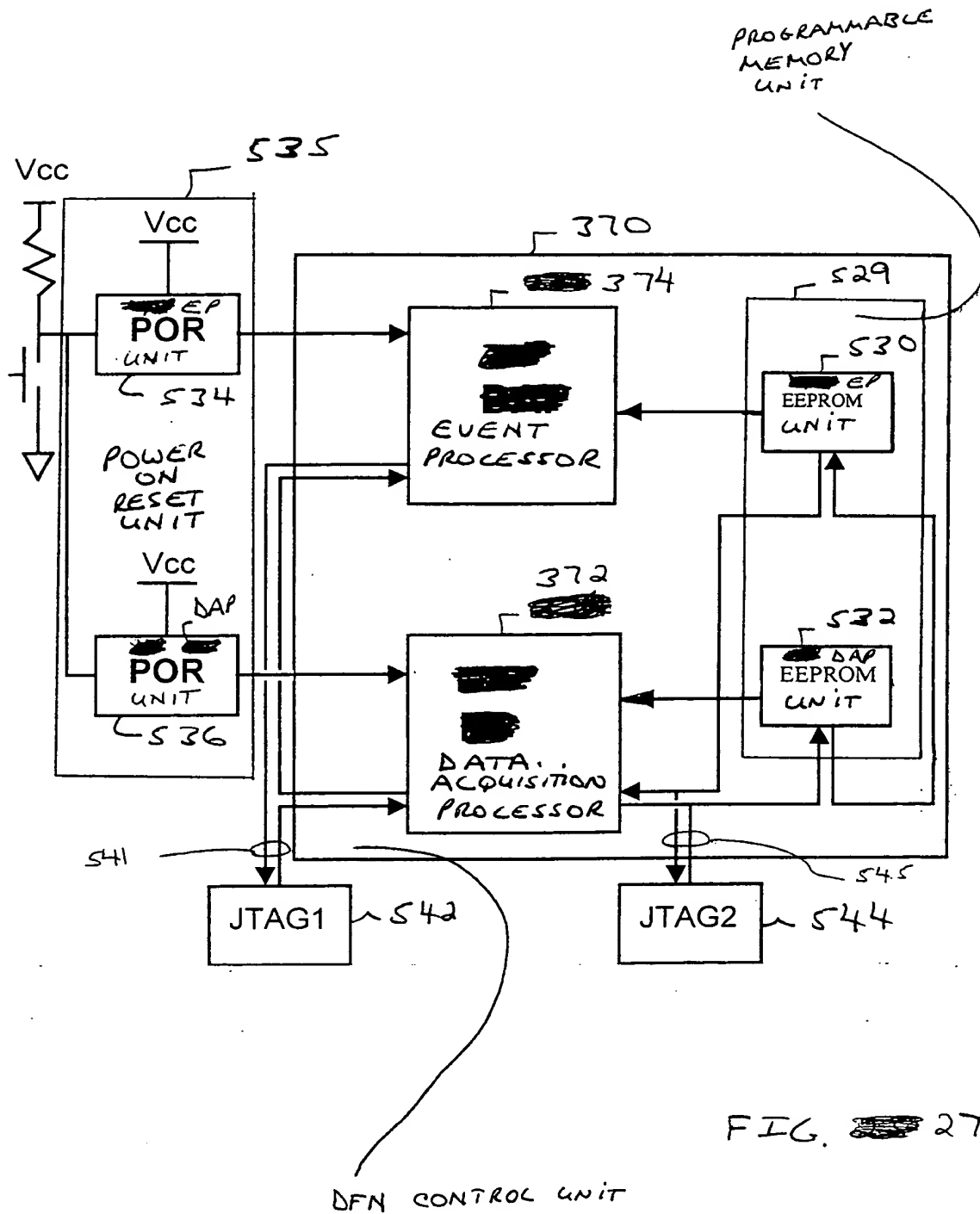


FIG. 27

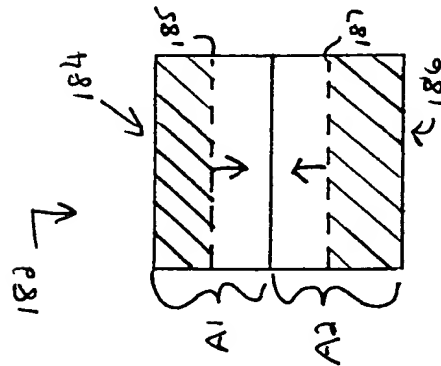


FIG. 28A  
28

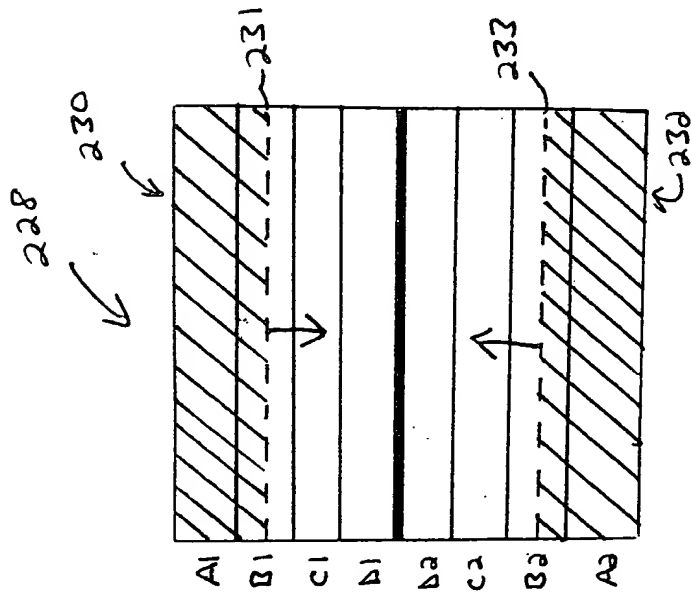


FIG. 29  
29

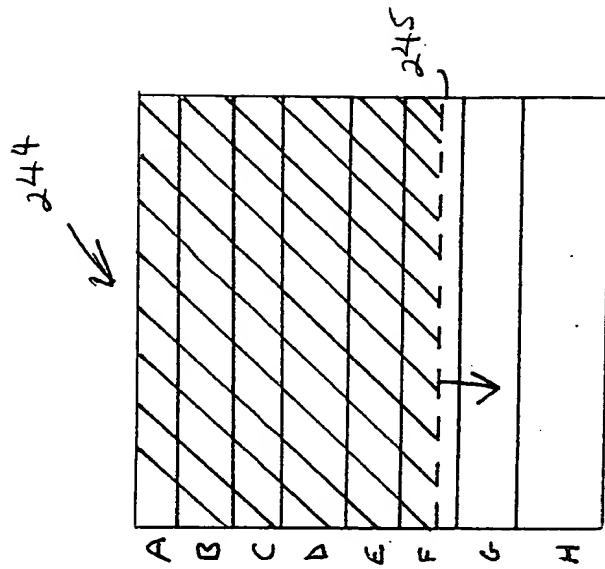


FIG. 30  
30

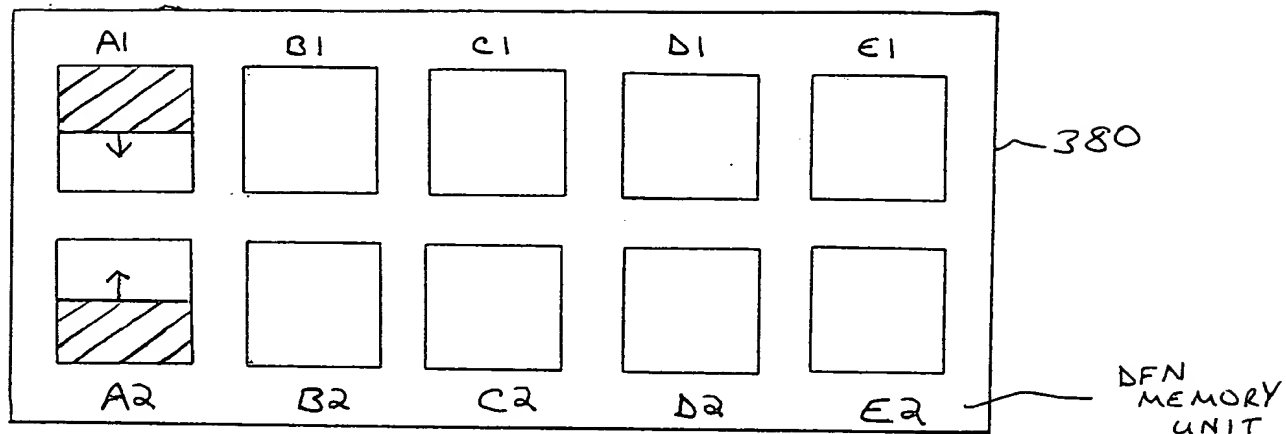


FIG. ~~30A~~ 31

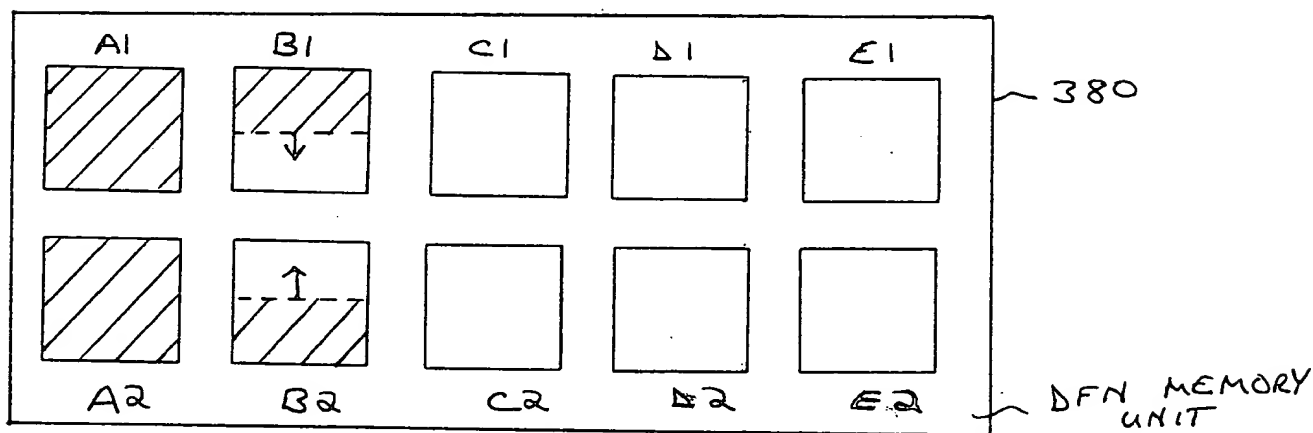


FIG. ~~30B~~ 32

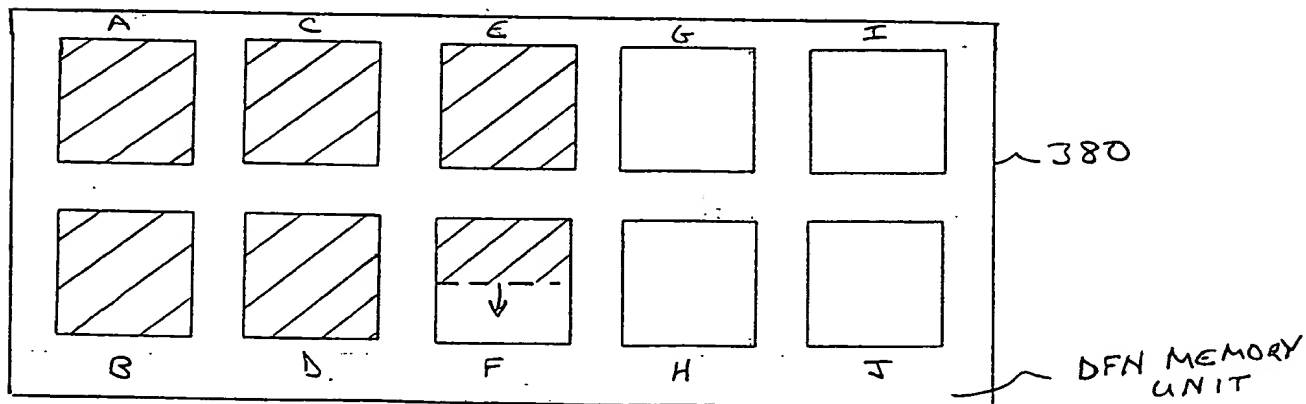


FIG. ~~30C~~ 33

3

334

A1
A2

FIG. ~~33A~~  
34

334

A1
<del>B1</del>
<del>C1</del>
A1
A2
C2
B2
A2

FIG. ~~33B~~  
35

334

A
B
C
D
E
F
G
H

FIG. ~~33C~~  
36

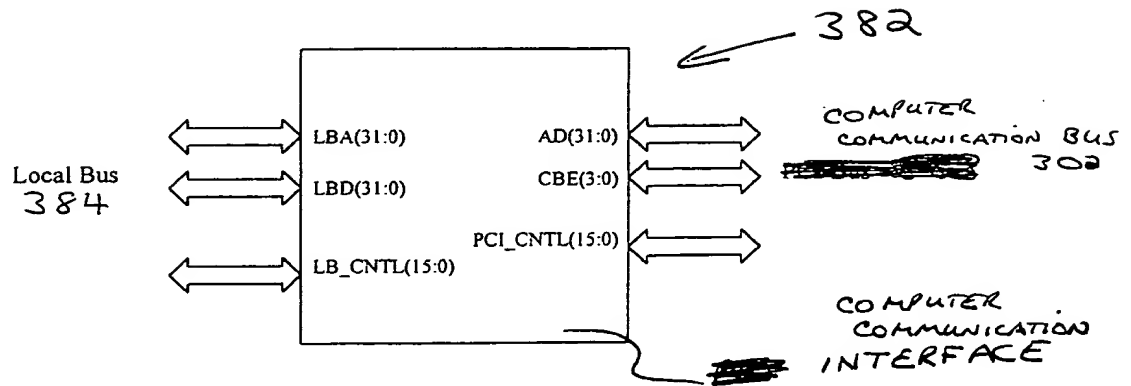


FIG. 37

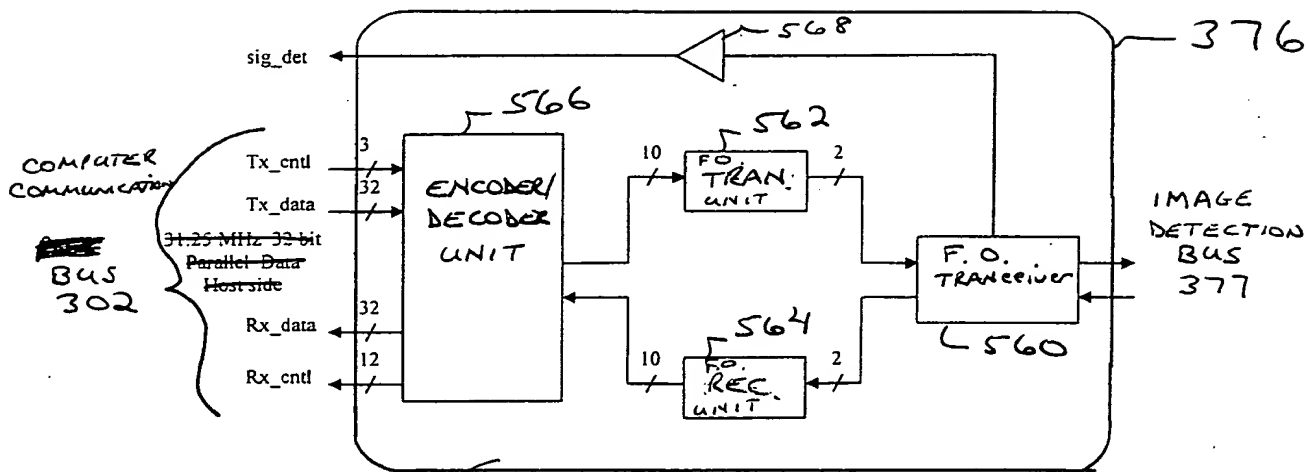


IMAGE DETECTION INTERFACE

FIG. 38

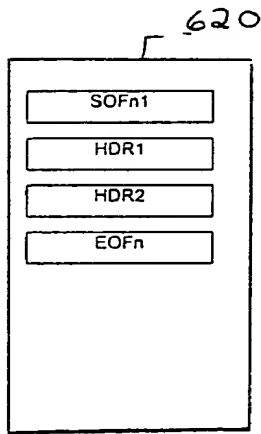


FIG. ~~38~~  
39

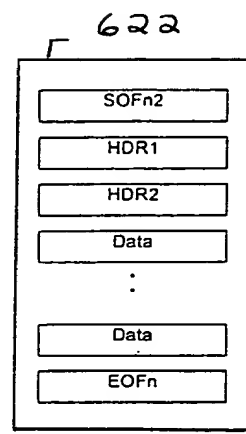


FIG. ~~39~~  
40

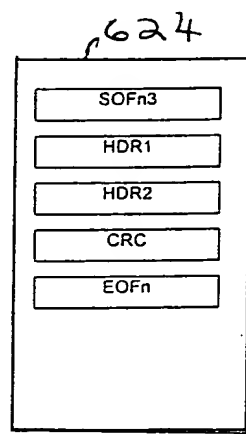


FIG. ~~40~~  
41



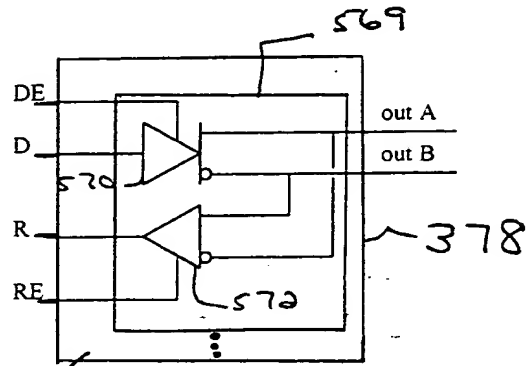
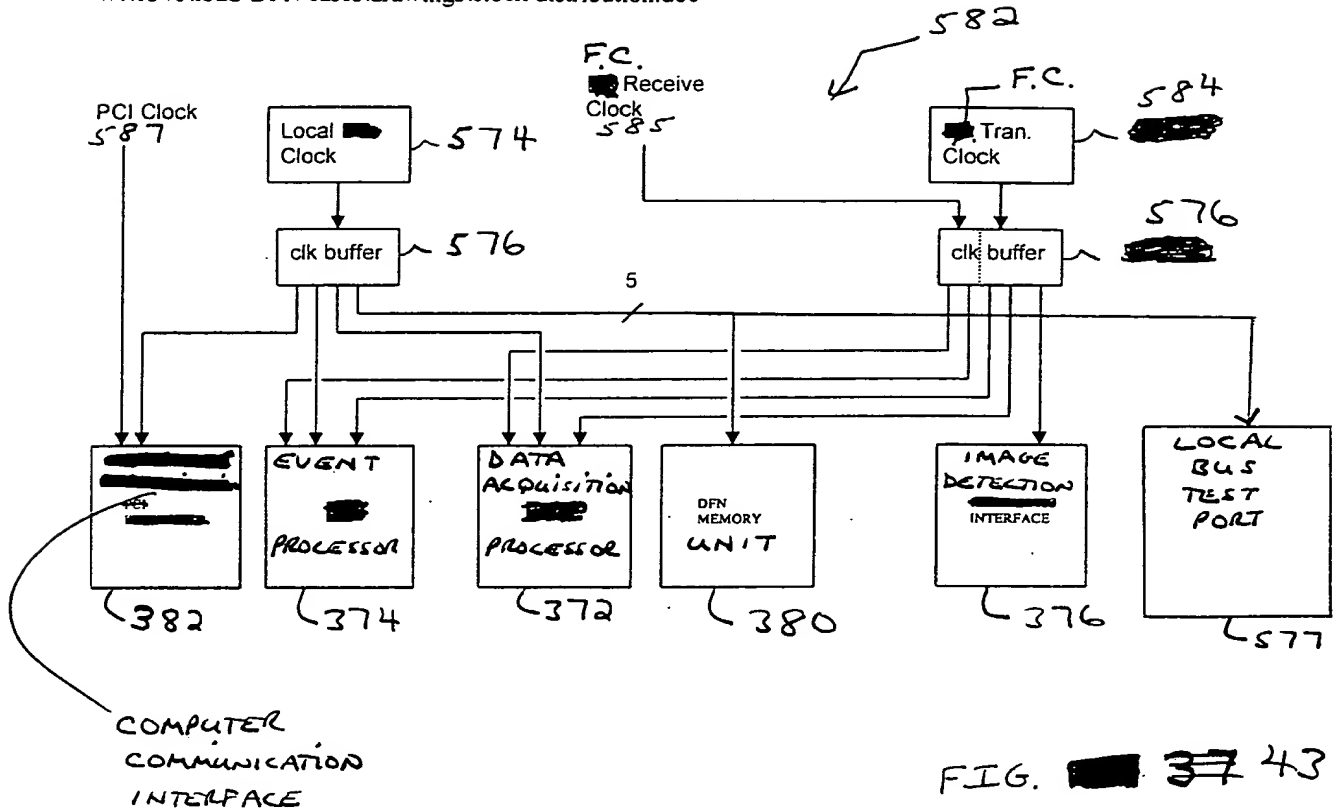


FIG. ~~41~~ ~~42~~ 42

REAL TIME  
BUS INTERFACE



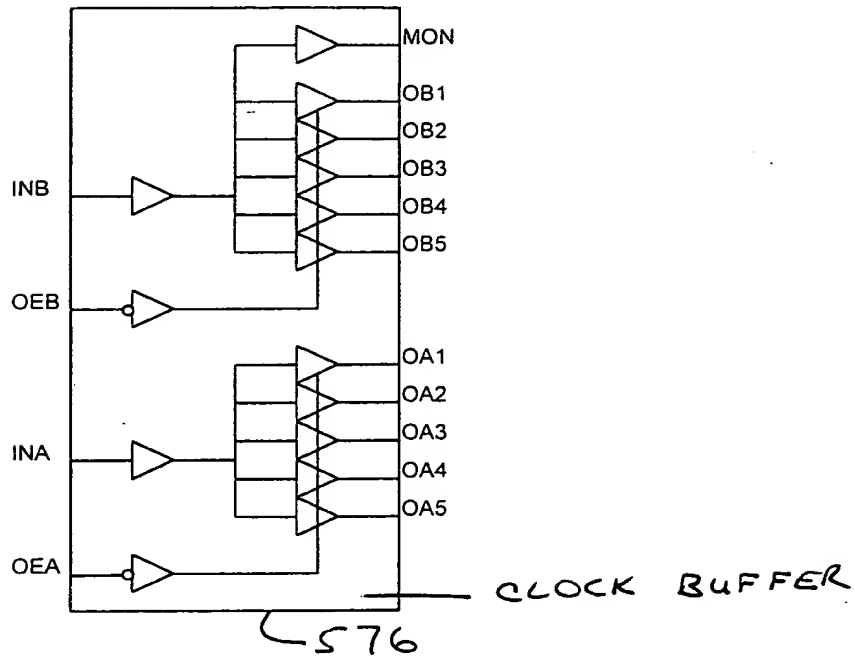


FIG. ~~44~~ 44

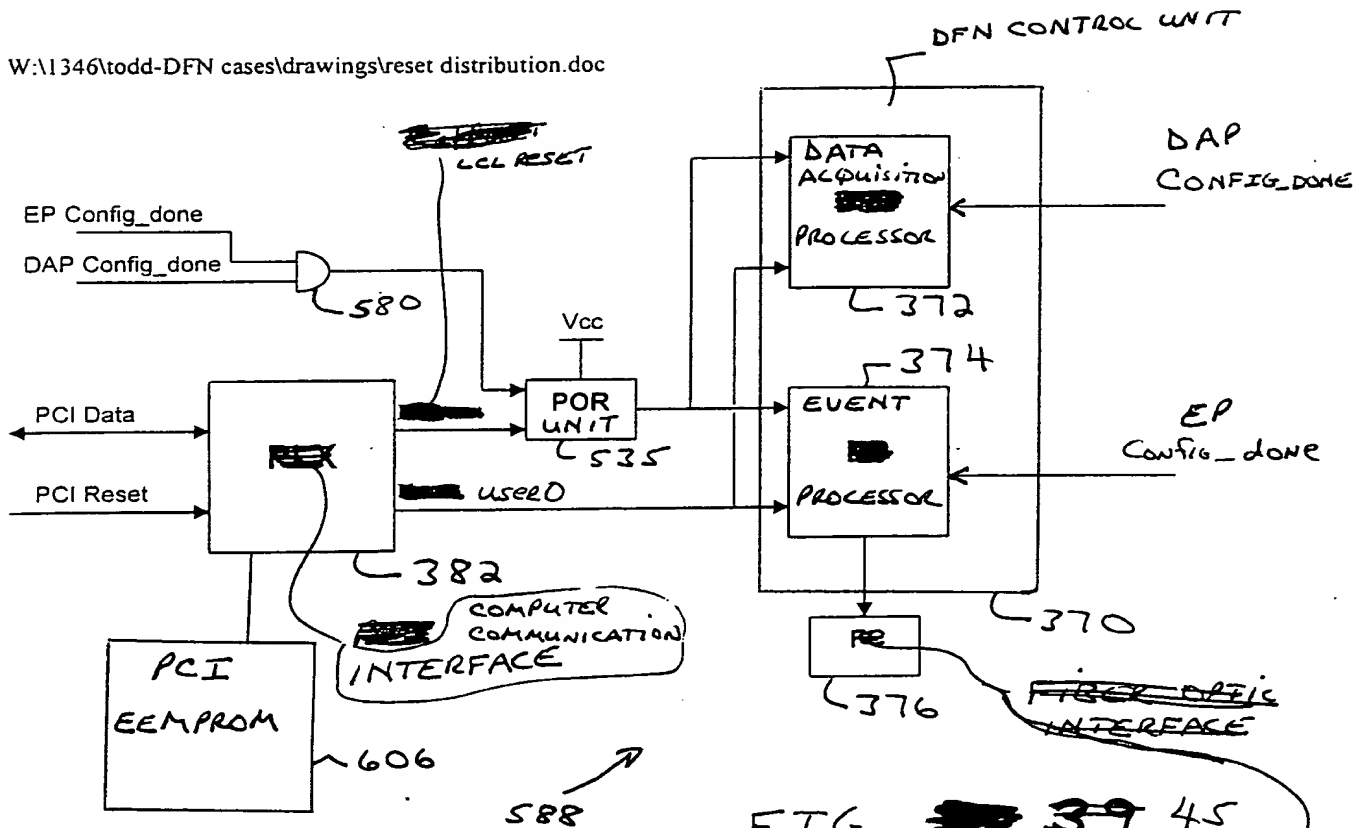


FIG. ~~39~~ 45

IMAGE DETECTION INTERFACE  
COMPUTER COMMUNICATION INTERFACE

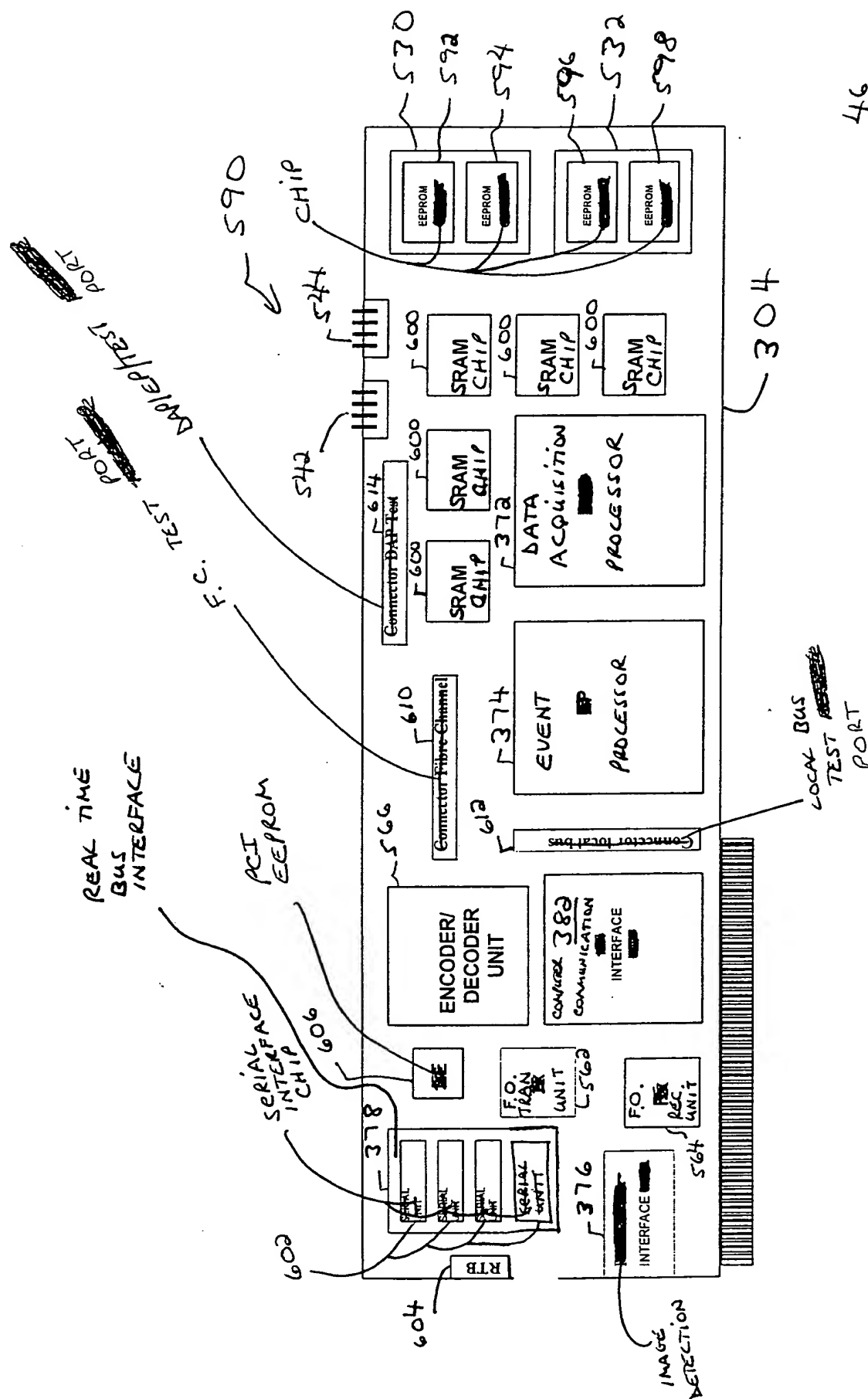
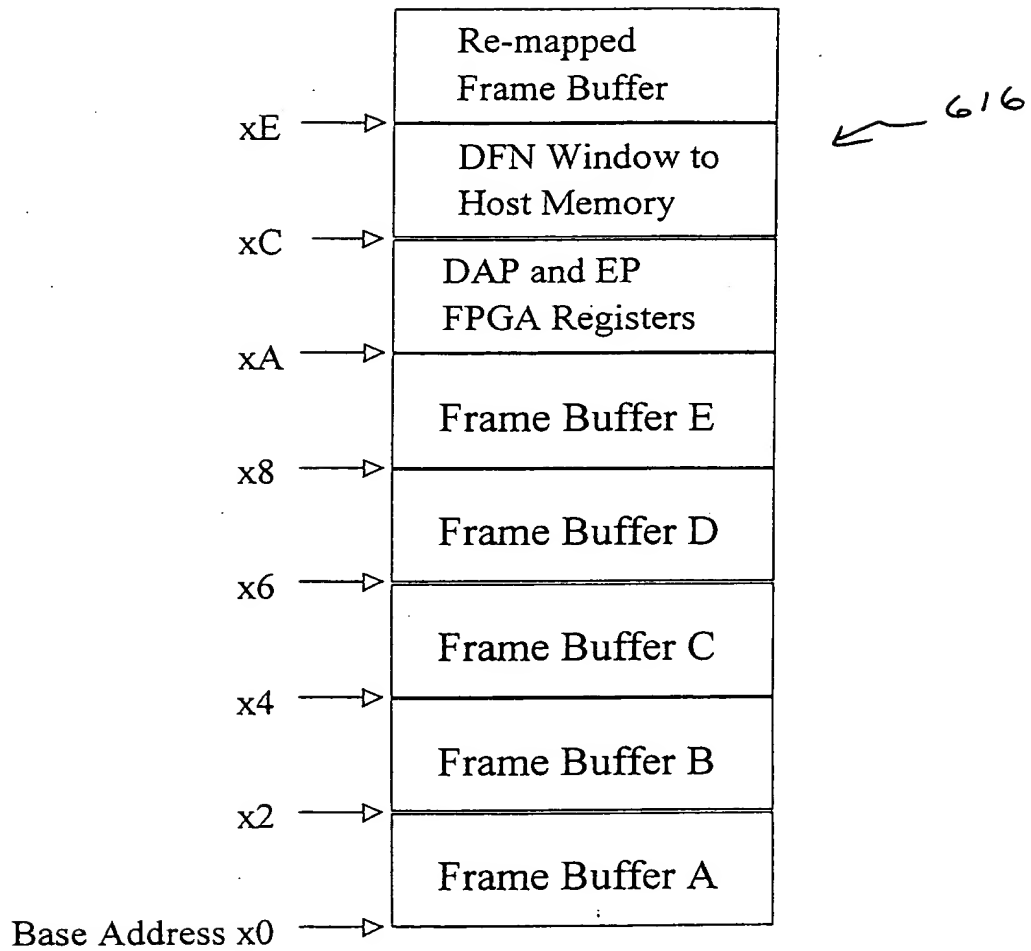


Fig.

46 ~~40~~



Mapping of 16 MByte PCI Address Space

FIG. 47

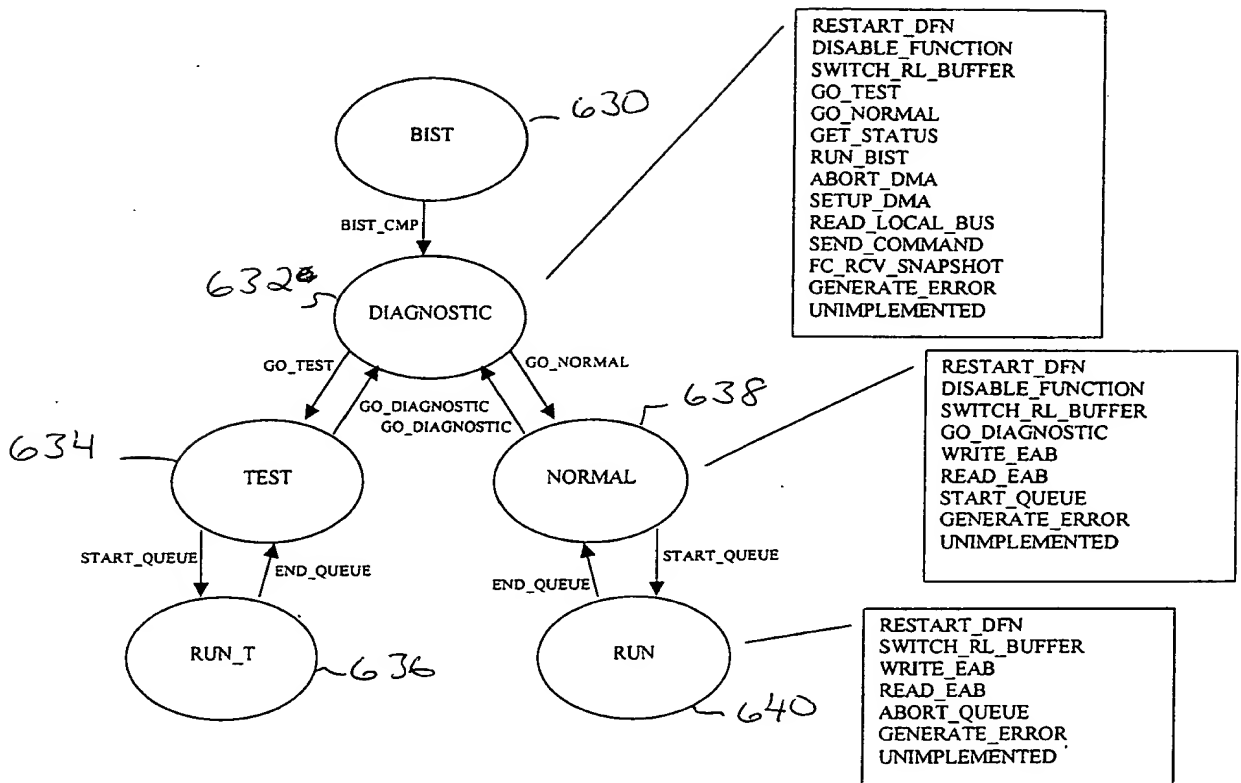


FIG. 48

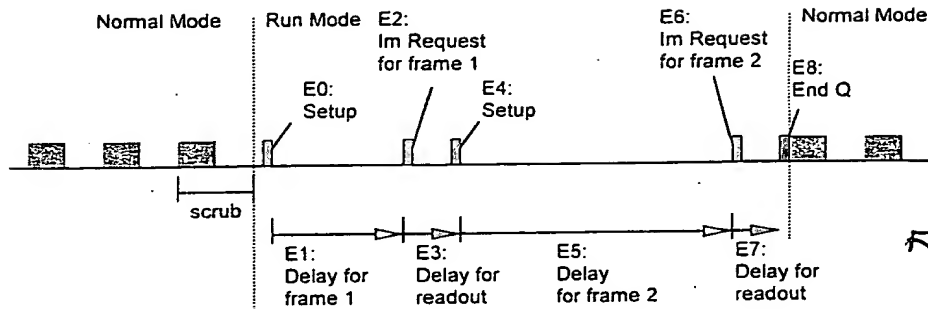


FIG. 49

Event Mnemonic	Event (showing size of arguments)	Op Code (hex)	Data (bytes)	Total (bytes)
Endq	Endq	14	0	1
Delay (I)	Delay (0xff ff ff ff)	10	4	5
Send (command, value)	Send (0xff ff ff ff, 0xff ff ff ff)	04	8	9
LoopKN (K, N)	LoopKN (0xff ff, 0xff)	0C	3	4
LoopKF (K, F)	LoopKF (0xff ff, 0xff ff ff)	0D	5	6
Wait (F)	Wait (0xff ff ff)	09	3	4
Flag (F)	Flag (0xff ff ff)	08	3	4

Handwritten note: ~670

FIG. 50

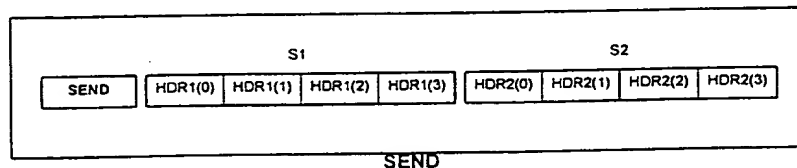


FIG. 51



Error Mnemonic	Description of Error
FC_TIMEOUT	Timeout expired with no ACK detected
FC_BAD_ACK	ACK did not match transmitted command
FC_EXTRA_ACK	Unexpected ACK received
FC_EXTRA_CMD	New Send event while waiting for ACK from previous Send
SIG_DETIN	No input signal power on Fibre Channel (cable disconnected?)
RXERROR	Fibre Channel receiver detected bad data (defective chipset?)
WRDSYNCHN	Fibre Channel Data link unsynchronized
CRXS(1)	Bad Received CRC detected (Fiber-optic cable problem?)
CRXS(3) and CRXS(2)	Bad order in link state machine (defective chipset?)

FIG. 52

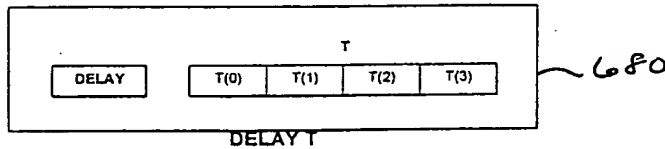


FIG. 53

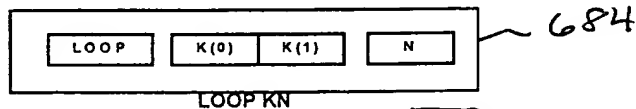


FIG. 54

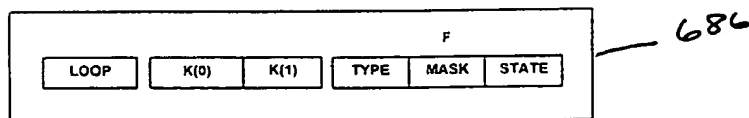
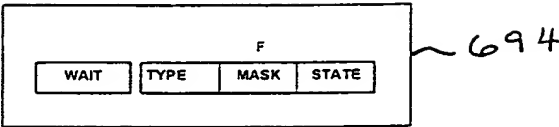
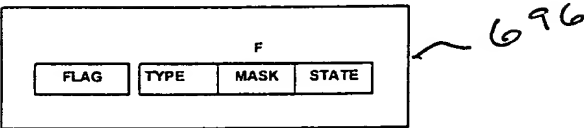


FIG. 55



WAIT F

FIG. 56



FLAG F

FIG. 57



FIG. 58

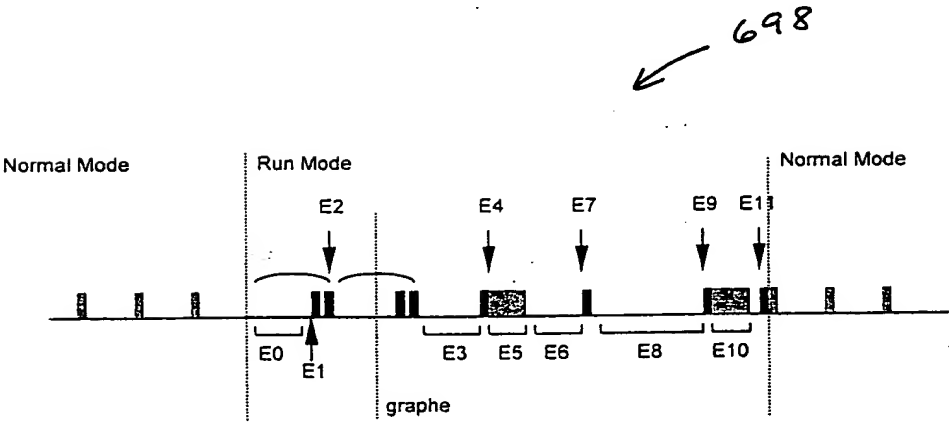


FIG. 59

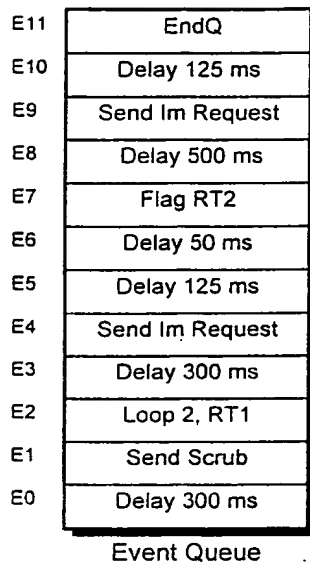


FIG. ~~60~~ 60

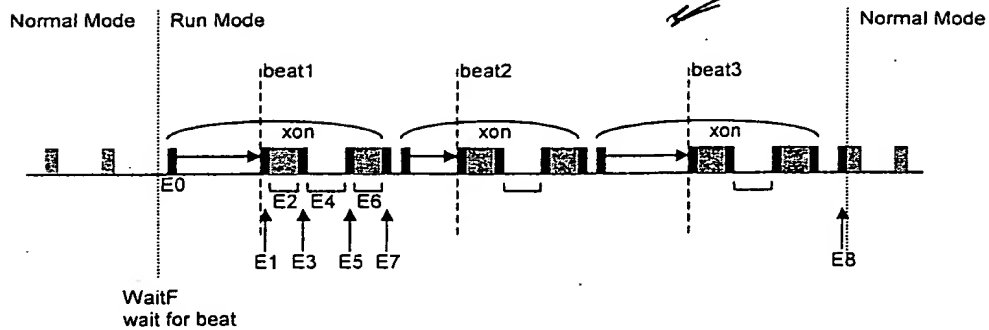
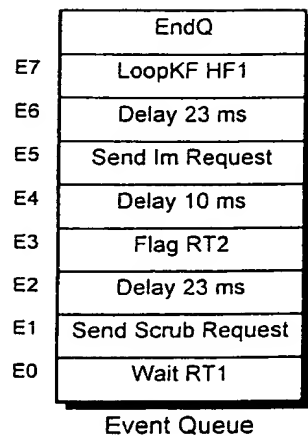


FIG. ~~61~~ 61



Event Queue

FIG. 62

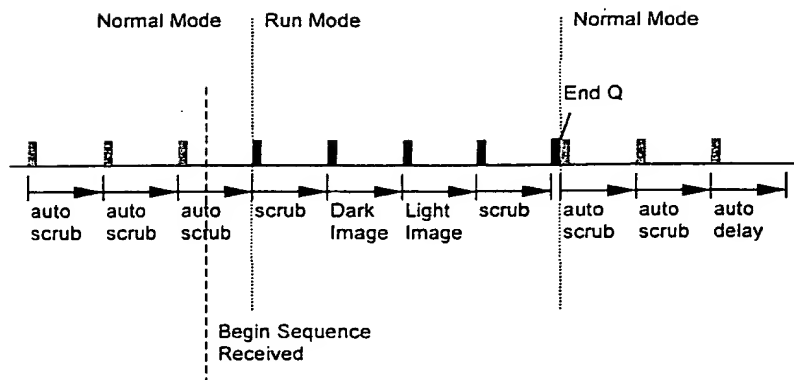


FIG. 63

```
sequence_begin ();

# define qv defaults:
%qv1 = ('delay_qv' => 5000);

# call frame with qv's
frame_type1 (NULL, \%qv1, 1);

sequence_end ();
```

FIG. 64

```
sub frame
{
    $QVf = 'frame';

    %qv = ('delay_qv' => [10000]);
    %qp = ();

    compile_init(@_, \%qp, \%qv, $QVf);

    Delay('delay_qv');

    compile_finit();
}
```

FIG. 65

```
pDFN->DFNChangeQueueVariable
(
    (char *)SymName,      // variable name
    (char *)sndBuf,      // new value
    BufSize,             // num bytes to write
    (ULONG *)&debug     // developer info
);
```

FIG. 66

**User Application**

```
// load and run the event sequence
pDFN->DFNBeginSequenceNoMappingNoLog
(snum, "d:\\HF.bin");

// assign data to be passed
sndBuf = 25000;

// change the queue variable
pDFN->DFNChangeQueueVariable
(
    (char *)SymName,      // variable name
    (char *)sndBuf,      // new value
    (ULONG)sizeof sndBuf, // num bytes to write
    (ULONG *)&debug     // developer info
);
```

FIG. 67

**Perl Script**

```
sub frame_type1
{
    $HFfrm = 'frame_type1';

    %qv = ('delay_qv' => [20000] );
    %qp = ();

    $image_cmd = [0x800000, 0x0];

    compile_init(@_, \%qp, \%qv, $HFfrm);

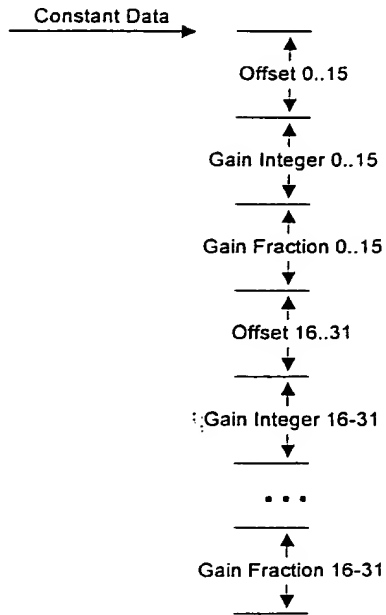
    Send($image_cmd);
    Delay('delay_qv');
    LoopKF(2, 0xAAFF01);

    compile_finit();
}
```

FIG. 68



44



Constant Memory Format

FIG.

~~70~~  
~~70~~  
~~70~~  
70

54

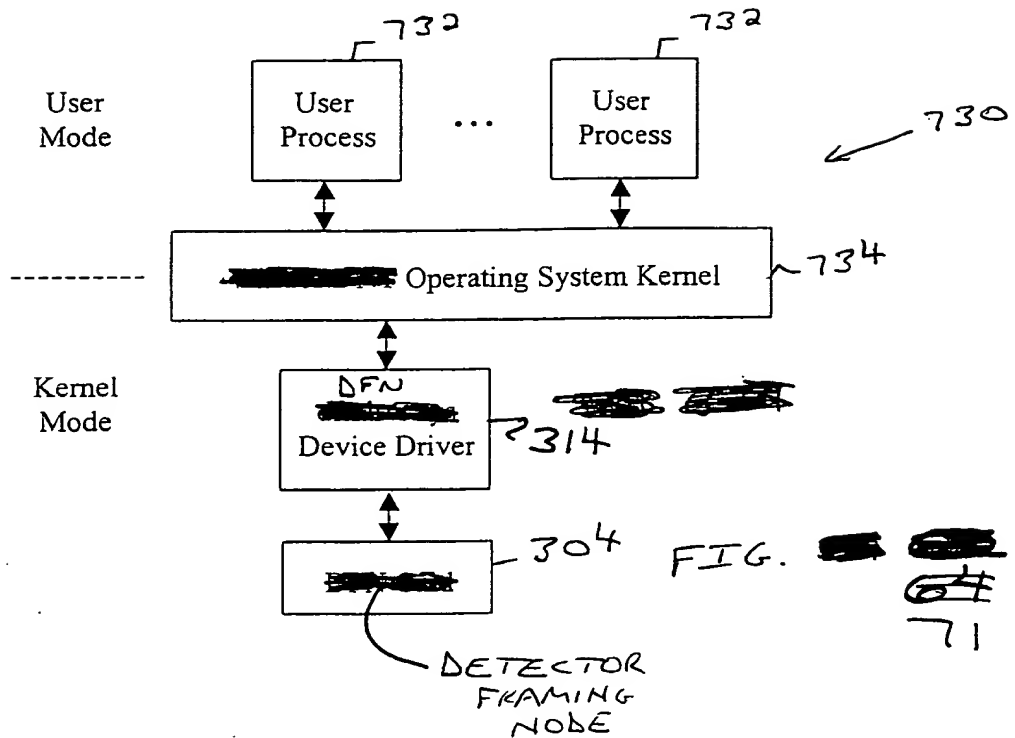


FIG. ~~64~~ 71

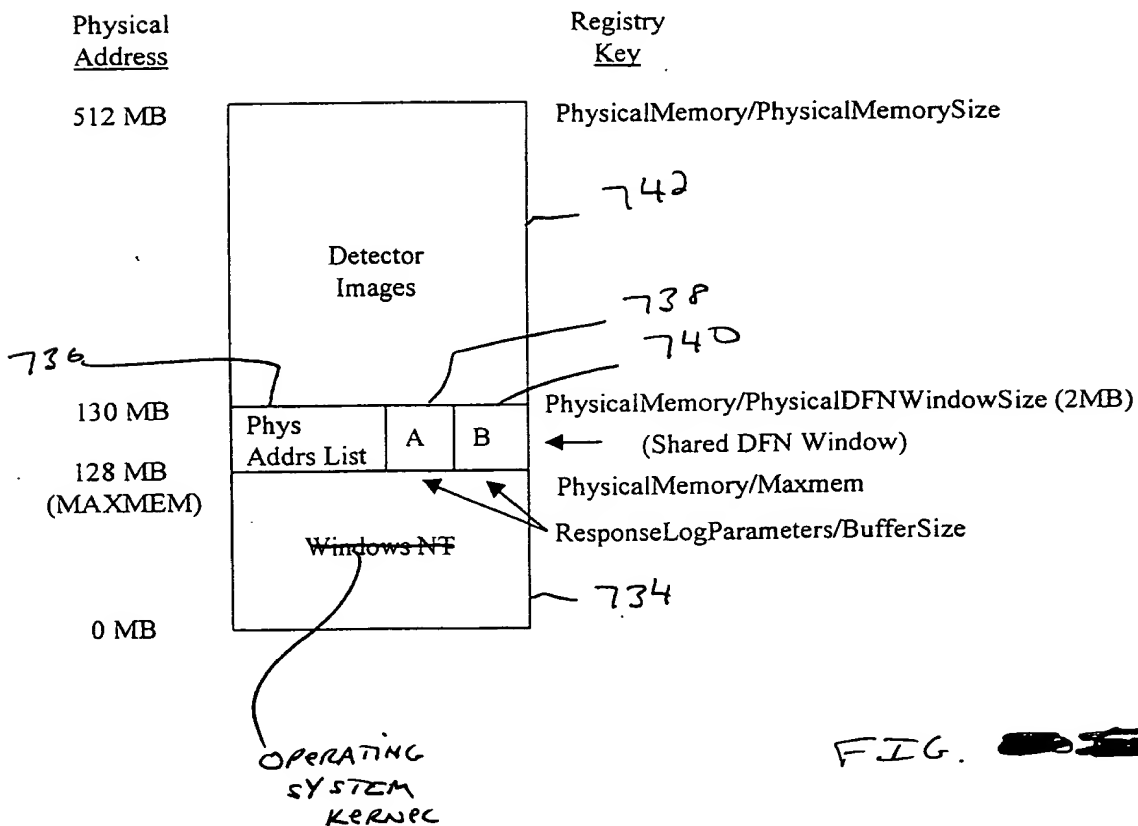


FIG. ~~64~~ 72



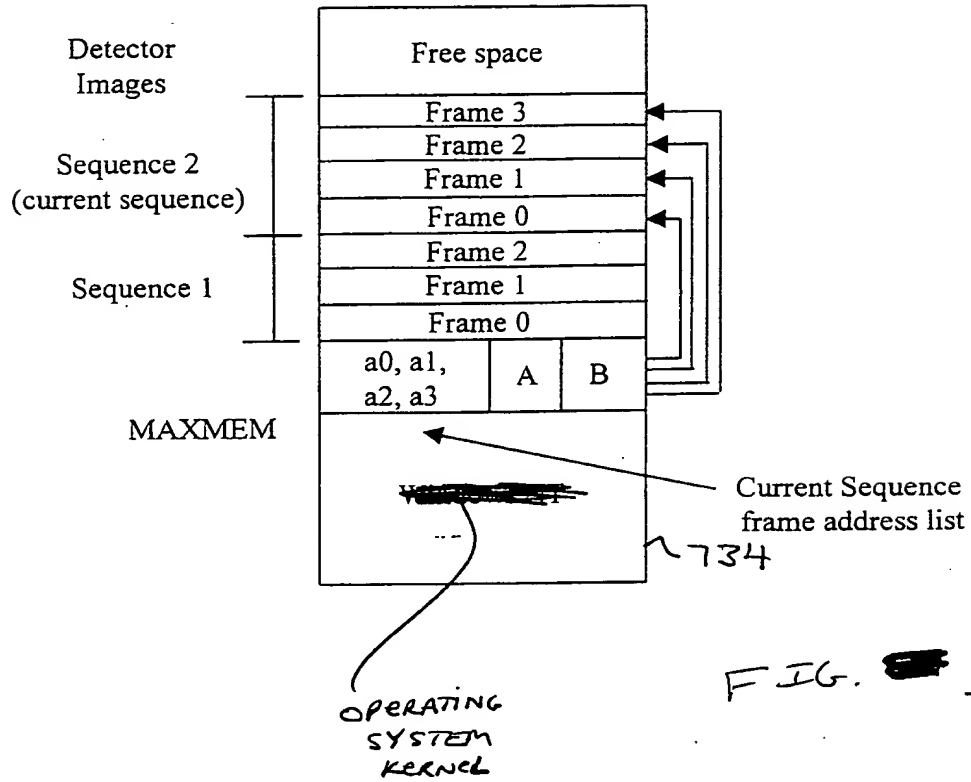


FIG. 73